

CBPR (RIGHT HAND) TABLE OF CONTENTS

PAGE	DESCRIPTION
CBPR. 1	TABLE OF CONTENTS
CBPR. 2-6	NMB CONNECTOR
CBPR. 7-11	NSP CONNECTOR
CBPR. 12-16	NVP CONNECTOR
CBPR. 17	P11 CONNECTOR
CBPR. 18	P12 CONNECTOR
CBPR. 19	P13 CONNECTOR
CBPR. 20	CLOCK CONNECTOR, COP CHIP, AND COP CONNECTOR
CBPR. 21	SYNONYMS, SLOT ID

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AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB1 1P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=1

GROUND ALL PING ON THIS ROW!

- 101 1_101
- 102 1_102
- 103 1_103
- 104 1_104
- 105 1_105
- 106 1_106
- 107 1_107
- 108 1_108
- 109 1_109
- 110 1_110
- 111 1_111
- 112 1_112
- 113 1_113
- 114 1_114
- 115 1_115
- 116 1_116
- 117 1_117
- 118 1_118
- 119 1_119
- 120 1_120
- 121 1_121
- 122 1_122
- 123 1_123
- 124 1_124
- 125 1_125
- 126 1_126
- 127 1_127
- 128 1_128
- 129 1_129
- 130 1_130
- 131 1_131
- 132 1_132
- 133 1_133
- 134 1_134
- 135 1_135
- 136 1_136 BP_MB1.PORTID<3>
- 137 1_137 MB1_BP.LBD_INIT_OUT
- 138 1_138
- 139 1_139 BP_MB1.SLOTID<3>
- 140 1_140 CU_MB1.CLOCK_2X

- 201 1_201
- 202 1_202
- 203 1_203
- 204 1_204
- 205 1_205
- 206 1_206
- 207 1_207
- 208 1_208
- 209 1_209
- 210 1_210
- 211 1_211
- 212 1_212
- 213 1_213
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- 215 1_215
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- 219 1_219
- 220 1_220
- 221 1_221
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- 223 1_223
- 224 1_224
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- 226 1_226
- 227 1_227
- 228 1_228
- 229 1_229
- 230 1_230
- 231 1_231
- 232 1_232
- 233 1_233
- 234 1_234
- 235 1_235
- 236 1_236 BP_MB1.PORTID<2>
- 237 1_237 BP_MB1.LBD_INIT_IN
- 238 1_238
- 239 1_239 BP_MB1.SLOTID<2>
- 240 1_240 CU_MB1.CLOCK_2X*

- 301 1_301
- 302 1_302
- 303 1_303
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- 305 1_305
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- 331 1_331
- 332 1_332
- 333 1_333
- 334 1_334
- 335 1_335
- 336 1_336
- 337 1_337 BP_MB1.PORTID<1>
- 338 1_338
- 339 1_339 BP_MB1.SLOTID<1>
- 340 1_340

- 401 1_401
- 402 1_402
- 403 1_403
- 404 1_404
- 405 1_405
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- 426 1_426
- 427 1_427
- 428 1_428 NMC_BYPASS
- 429 1_429
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- 432 1_432
- 433 1_433
- 434 1_434
- 435 1_435
- 436 1_436
- 437 1_437 BP_MB1.PORTID<0>
- 438 1_438
- 439 1_439 BP_MB1.SLOTID<0>
- 440 1_440

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TITLE: CBPR
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 PAGE: 2 of 21

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1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB1 1P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=2

GROUND ALL PINS ON THIS ROW!

- 101 2_101
- 102 2_102
- 103 2_103
- 104 2_104
- 105 2_105
- 106 2_106
- 107 2_107
- 108 2_108
- 109 2_109
- 110 2_110
- 111 2_111
- 112 2_112
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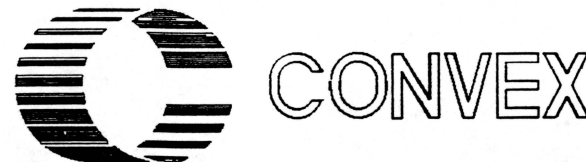
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PAGE: 3 of 21

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2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB1 1P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=3

GROUND ALL PINS ON THIS ROW!

101	3_101
102	3_102
103	3_103
104	3_104
105	3_105
106	3_106
107	3_107
108	3_108
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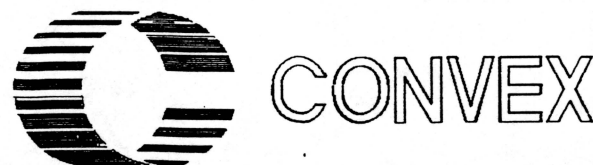
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PAGE: 4 of 21

8

7

6

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2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB1 154P
 BOARD=NMD

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=4

GROUND ALL PINS ON THIS ROW!

<p>101 4_101 XSO_MB1.ADDR<10> 102 4_102 XSO_MB1.ADDR<9> 103 4_103 104 4_104 105 4_105 XSO_MB1.WR_DATA<9> 106 4_106 XSO_MB1.WR_DATA<25> 107 4_107 XSO_MB1.WR_DATA<10> 108 4_108 XSO_MB1.WR_DATA<26> 109 4_109 XSO_MB1.WR_DATA<13> 110 4_110 XSO_MB1.WR_DATA<29> 111 4_111 XSO_MB1.WR_DATA<14> 112 4_112 XSO_MB1.WR_DATA<30> 113 4_113 XSO_MB1.WR_DATA<15> 114 4_114 XSO_MB1.WR_DATA<31> 115 4_115 XSO_MB1.WR_DATA<11> 116 4_116 XSO_MB1.WR_DATA<27> 117 4_117 XSO_MB1.WR_DATA<12> 118 4_118 XSO_MB1.WR_DATA<28> 119 4_119 XSO_MB1.WR_PAR<1> 120 4_120 XSO_MB1.WR_PAR<3> 121 4_121 96P 122 4_122 123 4_123 124 4_124 125 4_125 MB1_XSO.BANK_DONE<15..8> 126 4_126 127 4_127 128 4_128 129 4_129 130 4_130 131 4_131 132 4_132 133 4_133 XSOE_MB1.SPARE1 134 4_134 XSOE_MB1.SPARE0 135 4_135 XSIE_MB1.SPARE1 136 4_136 XSIE_MB1.SPARE0 137 4_137 MB1_XSIO.SEND_PAR_ERR 138 4_138 MB1_XSIO.SEND_PAR_ERR 139 4_139 MB1_XSOE.SEND_PAR_ERR 140 4_140 MB1_XSO0.SEND_PAR_ERR</p>	<p>201 4_201 XSO_MB1.WR_DATA<8> 202 4_202 XSO_MB1.WR_DATA<16> 203 4_203 XSO_MB1.WR_DATA<24> 204 4_204 XSO_MB1.WR_DATA<1> 205 4_205 XSO_MB1.WR_DATA<17> 206 4_206 XSO_MB1.WR_DATA<2> 207 4_207 XSO_MB1.WR_DATA<18> 208 4_208 XSO_MB1.WR_DATA<5> 209 4_209 XSO_MB1.WR_DATA<21> 210 4_210 XSO_MB1.WR_DATA<6> 211 4_211 XSO_MB1.WR_DATA<22> 212 4_212 XSO_MB1.WR_DATA<7> 213 4_213 XSO_MB1.WR_DATA<23> 214 4_214 XSO_MB1.WR_DATA<3> 215 4_215 XSO_MB1.WR_DATA<19> 216 4_216 XSO_MB1.WR_DATA<4> 217 4_217 XSO_MB1.WR_DATA<20> 218 4_218 XSO_MB1.WR_PAR<0> 219 4_219 XSO_MB1.WR_PAR<2> 220 4_220 221 4_221 145P 222 4_222 223 4_223 224 4_224 225 4_225 MB1_XSO.BANK_DONE<7..0> 226 4_226 227 4_227 228 4_228 229 4_229 230 4_230 231 4_231 232 4_232 233 4_233 234 4_234 235 4_235 236 4_236 237 4_237 238 4_238 239 4_239 M_CST.CERR_E 240 4_240 M_CST.CERR_O</p>	<p>301 4_301 XSE_MB1.ADDR<10> 302 4_302 XSE_MB1.ADDR<9> 303 4_303 304 4_304 305 4_305 XSE_MB1.WR_DATA<9> 306 4_306 XSE_MB1.WR_DATA<25> 307 4_307 XSE_MB1.WR_DATA<10> 308 4_308 XSE_MB1.WR_DATA<26> 309 4_309 XSE_MB1.WR_DATA<13> 310 4_310 XSE_MB1.WR_DATA<29> 311 4_311 XSE_MB1.WR_DATA<14> 312 4_312 XSE_MB1.WR_DATA<30> 313 4_313 XSE_MB1.WR_DATA<15> 314 4_314 XSE_MB1.WR_DATA<31> 315 4_315 XSE_MB1.WR_DATA<11> 316 4_316 XSE_MB1.WR_DATA<27> 317 4_317 XSE_MB1.WR_DATA<12> 318 4_318 XSE_MB1.WR_DATA<28> 319 4_319 XSE_MB1.WR_PAR<1> 320 4_320 XSE_MB1.WR_PAR<3> 321 4_321 128P 322 4_322 323 4_323 324 4_324 325 4_325 MB1_XSE.BANK_DONE<15..8> 326 4_326 327 4_327 328 4_328 329 4_329 330 4_330 331 4_331 XC_MB1.RAM_RFSH 332 4_332 333 4_333 XSE_MB1.REF_REQ 334 4_334 XSO_MB1.REF_REQ 335 4_335 336 4_336 337 4_337 MB1_XC.SOFT_ERROR 338 4_338 339 4_339 340 4_340</p>	<p>401 4_401 XSE_MB1.WR_DATA<8> 402 4_402 XSE_MB1.WR_DATA<16> 403 4_403 XSE_MB1.WR_DATA<24> 404 4_404 XSE_MB1.WR_DATA<1> 405 4_405 XSE_MB1.WR_DATA<17> 406 4_406 XSE_MB1.WR_DATA<2> 407 4_407 XSE_MB1.WR_DATA<18> 408 4_408 XSE_MB1.WR_DATA<5> 409 4_409 XSE_MB1.WR_DATA<21> 410 4_410 XSE_MB1.WR_DATA<6> 411 4_411 XSE_MB1.WR_DATA<22> 412 4_412 XSE_MB1.WR_DATA<7> 413 4_413 XSE_MB1.WR_DATA<23> 414 4_414 XSE_MB1.WR_DATA<3> 415 4_415 XSE_MB1.WR_DATA<19> 416 4_416 XSE_MB1.WR_DATA<4> 417 4_417 XSE_MB1.WR_DATA<20> 418 4_418 XSE_MB1.WR_PAR<0> 419 4_419 XSE_MB1.WR_PAR<2> 420 4_420 421 4_421 129P 422 4_422 423 4_423 424 4_424 425 4_425 MB1_XSE.BANK_DONE<7..0> 426 4_426 427 4_427 428 4_428 429 4_429 430 4_430 431 4_431 432 4_432 433 4_433 XSO0_MB1.SPARE1 434 4_434 XSO0_MB1.SPARE0 435 4_435 XSIO_MB1.SPARE1 436 4_436 XSIO_MB1.SPARE0 437 4_437 XC_MB1.SYS_RUNK 438 4_438 XC_MB1.SYS_RUNK 439 4_439 XC_MB1.LOG_RUNK 440 4_440</p>	<p>501 4_501 502 4_502 503 4_503 504 4_504 505 4_505 506 4_506 507 4_507 508 4_508 509 4_509 510 4_510 511 4_511 512 4_512 513 4_513 514 4_514 515 4_515 516 4_516 517 4_517 518 4_518 519 4_519 520 4_520 521 4_521 522 4_522 523 4_523 524 4_524 525 4_525 526 4_526 527 4_527 528 4_528 529 4_529 530 4_530 531 4_531 532 4_532 533 4_533 534 4_534 535 4_535 536 4_536 537 4_537 538 4_538 539 4_539 540 4_540</p>
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 PAGE: 5 of 21

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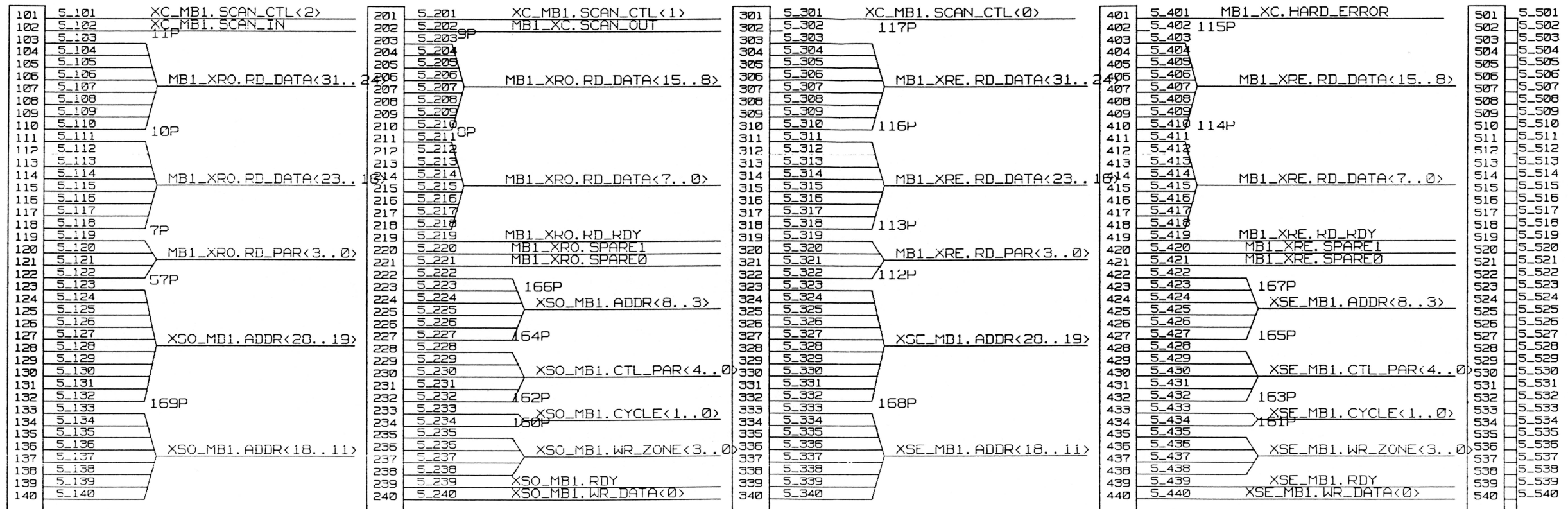
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AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB1 174P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=5

GROUND ALL PINS ON THIS ROW!



GND\G

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TITLE: CBPR
 DRAWING: 411-001207-300A REV 0.0
 REVISED: Thu Aug 16 20:45:31 1990

ABBR: CBPR
 ENGR: GOLENBIESKI

PAGE: 6 of 21

8

7

6

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1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP1 82P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=1

GROUND ALL PINS ON THIS ROW!

101	1.101	201	1.201	301	1.301 VP1_SP1.IDLE	401	1.401 SP1_VP1.DISP_EP<10>	501	1.501
102	1.102	202	1.202	302	1.302	402	1.402 SP1_VP1.DISP_EP<9>	502	1.502
103	1.103	203	1.203	303	1.303	403	1.403 SP1_VP1.DISP_EP<8>	503	1.503
104	1.104	204	1.204	304	1.304	404	1.404 SP1_VP1.DISP_EP<7>	504	1.504
105	1.105	205	1.205	305	1.305	405	1.405 SP1_VP1.DISP_EP<6>	505	1.505
106	1.106	206	1.206	306	1.306	406	1.406 SP1_VP1.DISP_EP<5>	506	1.506
107	1.107	207	1.207	307	1.307	407	1.407 SP1_VP1.DISP_EP<4>	507	1.507
108	1.108	208	1.208	308	1.308	408	1.408 SP1_VP1.DISP_EP<3>	508	1.508
109	1.109	209	1.209	309	1.309	409	1.409 SP1_VP1.DISP_EP<2>	509	1.509
110	1.110	210	1.210	310	1.310	410	1.410 SP1_VP1.DISP_EP<1>	510	1.510
111	1.111	211	1.211	311	1.311	411	1.411 SP1_VP1.DISP_EP<0>	511	1.511
112	1.112	212	1.212	312	1.312	412	1.412 SP1_VP1.DISP_IREG<2>	512	1.512
113	1.113	213	1.213	313	1.313	413	1.413 SP1_VP1.DISP_IREG<1>	513	1.513
114	1.114	214	1.214	314	1.314	414	1.414 SP1_VP1.DISP_IREG<0>	514	1.514
115	1.115	215	1.215	315	1.315	415	1.415 SP1_VP1.DISP_JREG<2>	515	1.515
116	1.116	216	1.216	316	1.316	416	1.416 SP1_VP1.DISP_JREG<1>	516	1.516
117	1.117	217	1.217	317	1.317	417	1.417 SP1_VP1.DISP_JREG<0>	517	1.517
118	1.118	218	1.218	318	1.318	418	1.418 SP1_VP1.DISP_KREG<2>	518	1.518
119	1.119	219	1.219	319	1.319	419	1.419 SP1_VP1.DISP_KREG<1>	519	1.519
120	1.120	220	1.220	320	1.320	420	1.420 SP1_VP1.DISP_KREG<0>	520	1.520
121	1.121	221	1.221	321	1.321	421	1.421	521	1.521
122	1.122	222	1.222	322	1.322	422	1.422 SP1_VP1.IEEE	522	1.522
123	1.123	223	1.223	323	1.323	423	1.423	523	1.523
124	1.124	224	1.224	324	1.324	424	1.424	524	1.524
125	1.125	225	1.225	325	1.325	425	1.425	525	1.525
126	1.126	226	1.226	326	1.326	426	1.426	526	1.526
127	1.127	227	1.227	327	1.327	427	1.427	527	1.527
128	1.128	228	1.228	328	1.328	428	1.428	528	1.528
129	1.129	229	1.229	329	1.329	429	1.429	529	1.529
130	1.130	230	1.230	330	1.330	430	1.430	530	1.530
131	1.131	231	1.231	331	1.331	431	1.431	531	1.531
132	1.132	232	1.232	332	1.332	432	1.432	532	1.532
133	1.133	233	1.233	333	1.333	433	1.433	533	1.533
134	1.134	234	1.234	334	1.334	434	1.434	534	1.534
135	1.135	235	1.235	335	1.335	435	1.435	535	1.535
136	1.136 BP_SP1.PORTID<3>	236	1.236 BP_SP1.PORTID<2>	336	1.336	436	1.436	536	1.536
137	1.137 SP1_EP.LBD_INTL_CUT	237	1.237 EP_SP1.LBD_INTL_IN	337	1.337 BP_SP1.PORTID<1>	437	1.437 BP_SP1.PORTID<0>	537	1.537
138	1.138	238	1.238	338	1.338	438	1.438	538	1.538
139	1.139 BP_SP1.SLOTID<3>	239	1.239 BP_SP1.SLOTID<2>	339	1.339 BP_SP1.SLOTID<1>	439	1.439 BP_SP1.SLOTID<0>	539	1.539
140	1.140 CU_SP1.CLOCK_2X	240	1.240 CU_SP1.CLOCK_2X*	340	1.340	440	1.440	540	1.540 GND\G

SECTION 1 (BOTTOM)

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 REVISID: Thu Aug 16 20:46:12 1990
 ABBR: CBPR
 ENGR: GOLENBIESKI
 PAGE: 7 of 21

8

7

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1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP1 90P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=2

GROUND ALL PINS ON THIS ROW!

101	2_101 XRO_SP1_RD_DATA<5>
102	2_102 XRO_SP1_RD_DATA<6>
103	2_103 XRO_SP1_RD_DATA<7>
104	2_104 XRO_SP1_RD_DATA<13>
105	2_105 XRO_SP1_RD_DATA<14>
106	2_106 XRO_SP1_RD_DATA<15>
107	2_107 XRO_SP1_RD_DATA<21>
108	2_108 XRO_SP1_RD_DATA<22>
109	2_109 XRO_SP1_RD_DATA<23>
110	2_110 XRO_SP1_RD_DATA<29>
111	2_111 XRO_SP1_RD_DATA<30>
112	2_112 XRO_SP1_RD_DATA<31>
113	2_113 XRE_SP1_RD_DATA<5>
114	2_114 XRE_SP1_RD_DATA<6>
115	2_115 XRE_SP1_RD_DATA<7>
116	2_116 XRE_SP1_RD_DATA<13>
117	2_117 XRE_SP1_RD_DATA<14>
118	2_118 XRE_SP1_RD_DATA<15>
119	2_119 XRE_SP1_RD_DATA<21>
120	2_120 XRE_SP1_RD_DATA<22>
121	2_121 XRE_SP1_RD_DATA<23>
122	2_122 XRE_SP1_RD_DATA<29>
123	2_123 XRE_SP1_RD_DATA<30>
124	2_124 XRE_SP1_RD_DATA<31>
125	2_125
126	2_126
127	2_127
128	2_128
129	2_129
130	2_130
131	2_131
132	2_132
133	2_133
134	2_134
135	2_135
136	2_136
137	2_137 VPI_SP1_SPARE3
138	2_138 VPI_SP1_SPARE2
139	2_139 VPI_SP1_SPARE1
140	2_140 VPI_SP1_SPARE0

201	2_201 SP1_XSO_WR_DATA<5>
202	2_202 SP1_XSO_WR_DATA<6>
203	2_203 SP1_XSO_WR_DATA<7>
204	2_204 SP1_XSO_WR_DATA<13>
205	2_205 SP1_XSO_WR_DATA<14>
206	2_206 SP1_XSO_WR_DATA<15>
207	2_207 SP1_XSO_WR_DATA<21>
208	2_208 SP1_XSO_WR_DATA<22>
209	2_209 SP1_XSO_WR_DATA<23>
210	2_210 SP1_XSO_WR_DATA<29>
211	2_211 SP1_XSO_WR_DATA<30>
212	2_212 SP1_XSO_WR_DATA<31>
213	2_213 SP1_XSE_WR_DATA<5>
214	2_214 SP1_XSE_WR_DATA<6>
215	2_215 SP1_XSE_WR_DATA<7>
216	2_216 SP1_XSE_WR_DATA<13>
217	2_217 SP1_XSE_WR_DATA<14>
218	2_218 SP1_XSE_WR_DATA<15>
219	2_219 SP1_XSE_WR_DATA<21>
220	2_220 SP1_XSE_WR_DATA<22>
221	2_221 SP1_XSE_WR_DATA<23>
222	2_222 SP1_XSE_WR_DATA<29>
223	2_223 SP1_XSE_WR_DATA<30>
224	2_224 SP1_XSE_WR_DATA<31>
225	2_225
226	2_226
227	2_227
228	2_228
229	2_229
230	2_230
231	2_231
232	2_232
233	2_233
234	2_234
235	2_235
236	2_236
237	2_237
238	2_238
239	2_239
240	2_240

301	2_301 VPI_SP1_DATA<5>
302	2_302 VPI_SP1_DATA<6>
303	2_303 VPI_SP1_DATA<7>
304	2_304 VPI_SP1_DATA<13>
305	2_305 VPI_SP1_DATA<14>
306	2_306 VPI_SP1_DATA<15>
307	2_307 VPI_SP1_DATA<21>
308	2_308 VPI_SP1_DATA<22>
309	2_309 VPI_SP1_DATA<23>
310	2_310 VPI_SP1_DATA<29>
311	2_311 VPI_SP1_DATA<30>
312	2_312 VPI_SP1_DATA<31>
313	2_313 VPI_SP1_DATA<37>
314	2_314 VPI_SP1_DATA<38>
315	2_315 VPI_SP1_DATA<39>
316	2_316 VPI_SP1_DATA<45>
317	2_317 VPI_SP1_DATA<46>
318	2_318 VPI_SP1_DATA<47>
319	2_319 VPI_SP1_DATA<53>
320	2_320 VPI_SP1_DATA<54>
321	2_321 VPI_SP1_DATA<55>
322	2_322 VPI_SP1_DATA<61>
323	2_323 VPI_SP1_DATA<62>
324	2_324 VPI_SP1_DATA<63>
325	2_325
326	2_326
327	2_327
328	2_328
329	2_329
330	2_330 VPI_SP1_MXV_REQ_NEXT
331	2_331 VPI_SP1_SXV_REQ_NEXT
332	2_332
333	2_333 VPI_SP1_PSW_HAZ
334	2_334 VPI_SP1_SET_FDZ
335	2_335 VPI_SP1_SET_FSN
336	2_336 VPI_SP1_SET_OV
337	2_337 VPI_SP1_SET_RO
338	2_338 VPI_SP1_SET_SDZ
339	2_339 VPI_SP1_SET_SIV
340	2_340 VPI_SP1_SET_UN

401	2_401 SP1_VPI1_DATA<5>
402	2_402 SP1_VPI1_DATA<6>
403	2_403 SP1_VPI1_DATA<7>
404	2_404 SP1_VPI1_DATA<13>
405	2_405 SP1_VPI1_DATA<14>
406	2_406 SP1_VPI1_DATA<15>
407	2_407 SP1_VPI1_DATA<21>
408	2_408 SP1_VPI1_DATA<22>
409	2_409 SP1_VPI1_DATA<23>
410	2_410 SP1_VPI1_DATA<29>
411	2_411 SP1_VPI1_DATA<30>
412	2_412 SP1_VPI1_DATA<31>
413	2_413 SP1_VPI1_DATA<37>
414	2_414 SP1_VPI1_DATA<38>
415	2_415 SP1_VPI1_DATA<39>
416	2_416 SP1_VPI1_DATA<45>
417	2_417 SP1_VPI1_DATA<46>
418	2_418 SP1_VPI1_DATA<47>
419	2_419 SP1_VPI1_DATA<53>
420	2_420 SP1_VPI1_DATA<54>
421	2_421 SP1_VPI1_DATA<55>
422	2_422 SP1_VPI1_DATA<61>
423	2_423 SP1_VPI1_DATA<62>
424	2_424 SP1_VPI1_DATA<63>
425	2_425
426	2_426
427	2_427
428	2_428
429	2_429
430	2_430
431	2_431
432	2_432 SP1_VPI1_DISP_RDY
433	2_433 SP1_VPI1_DISP_PSW_HAZ
434	2_434
435	2_435
436	2_436
437	2_437
438	2_438
439	2_439
440	2_440

501	2_501
502	2_502
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506	2_506
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508	2_508
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510	2_510
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527	2_527
528	2_528
529	2_529
530	2_530
531	2_531
532	2_532
533	2_533
534	2_534
535	2_535
536	2_536
537	2_537
538	2_538
539	2_539
540	2_540 GND'NG

SECTION 2

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REVISED: Thu Aug 16 20:47:02 1990

PAGE: 8 of 21

8

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1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP1 77P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=3

GROUND ALL PINS ON THIS ROW!

101	3.101	XRO_SP1.RD_DATA<2>
102	3.102	XRO_SP1.RD_DATA<3>
103	3.103	XRO_SP1.RD_DATA<4>
104	3.104	XRO_SP1.RD_DATA<10>
105	3.105	XRO_SP1.RD_DATA<11>
106	3.106	XRO_SP1.RD_DATA<12>
107	3.107	XRO_SP1.RD_DATA<18>
108	3.108	XRO_SP1.RD_DATA<19>
109	3.109	XRO_SP1.RD_DATA<20>
110	3.110	XRO_SP1.RD_DATA<26>
111	3.111	XRO_SP1.RD_DATA<27>
112	3.112	XRO_SP1.RD_DATA<28>
113	3.113	XRE_SP1.RD_DATA<2>
114	3.114	XRE_SP1.RD_DATA<3>
115	3.115	XRE_SP1.RD_DATA<4>
116	3.116	XRE_SP1.RD_DATA<10>
117	3.117	XRE_SP1.RD_DATA<11>
118	3.118	XRE_SP1.RD_DATA<12>
119	3.119	XRE_SP1.RD_DATA<18>
120	3.120	XRE_SP1.RD_DATA<19>
121	3.121	XRE_SP1.RD_DATA<20>
122	3.122	XRE_SP1.RD_DATA<26>
123	3.123	XRE_SP1.RD_DATA<27>
124	3.124	XRE_SP1.RD_DATA<28>
125	3.125	
126	3.126	
127	3.127	
128	3.128	
129	3.129	
130	3.130	
131	3.131	
132	3.132	VP1_SP1.VXA_ADDR<0>
133	3.133	VP1_SP1.VXA_ADDR<24>
134	3.134	VP1_SP1.VXA_ADDR<25>
135	3.135	VP1_SP1.VXA_ADDR<26>
136	3.136	VP1_SP1.VXA_ADDR<27>
137	3.137	VP1_SP1.VXA_ADDR<28>
138	3.138	VP1_SP1.VXA_ADDR<29>
139	3.139	VP1_SP1.VXA_ADDR<30>
140	3.140	VP1_SP1.VXA_ADDR<31>

201	3.201	SP1_XSO.WR_DATA<2>
202	3.202	SP1_XSO.WR_DATA<3>
203	3.203	SP1_XSO.WR_DATA<4>
204	3.204	SP1_XSO.WR_DATA<10>
205	3.205	SP1_XSO.WR_DATA<11>
206	3.206	SP1_XSO.WR_DATA<12>
207	3.207	SP1_XSO.WR_DATA<18>
208	3.208	SP1_XSO.WR_DATA<19>
209	3.209	SP1_XSO.WR_DATA<20>
210	3.210	SP1_XSO.WR_DATA<26>
211	3.211	SP1_XSO.WR_DATA<27>
212	3.212	SP1_XSO.WR_DATA<28>
213	3.213	SP1_XSE.WR_DATA<2>
214	3.214	SP1_XSE.WR_DATA<3>
215	3.215	SP1_XSE.WR_DATA<4>
216	3.216	SP1_XSE.WR_DATA<10>
217	3.217	SP1_XSE.WR_DATA<11>
218	3.218	SP1_XSE.WR_DATA<12>
219	3.219	SP1_XSE.WR_DATA<18>
220	3.220	SP1_XSE.WR_DATA<19>
221	3.221	SP1_XSE.WR_DATA<20>
222	3.222	SP1_XSE.WR_DATA<26>
223	3.223	SP1_XSE.WR_DATA<27>
224	3.224	SP1_XSE.WR_DATA<28>
225	3.225	
226	3.226	
227	3.227	
228	3.228	
229	3.229	
230	3.230	
231	3.231	
232	3.232	VP1_SP1.VXA_ADDR<1>
233	3.233	VP1_SP1.VXA_ADDR<16>
234	3.234	VP1_SP1.VXA_ADDR<17>
235	3.235	VP1_SP1.VXA_ADDR<18>
236	3.236	VP1_SP1.VXA_ADDR<19>
237	3.237	VP1_SP1.VXA_ADDR<20>
238	3.238	VP1_SP1.VXA_ADDR<21>
239	3.239	VP1_SP1.VXA_ADDR<22>
240	3.240	VP1_SP1.VXA_ADDR<23>

301	3.301	VP1_SP1.DATA<2>
302	3.302	VP1_SP1.DATA<3>
303	3.303	VP1_SP1.DATA<4>
304	3.304	VP1_SP1.DATA<10>
305	3.305	VP1_SP1.DATA<11>
306	3.306	VP1_SP1.DATA<12>
307	3.307	VP1_SP1.DATA<18>
308	3.308	VP1_SP1.DATA<19>
309	3.309	VP1_SP1.DATA<20>
310	3.310	VP1_SP1.DATA<26>
311	3.311	VP1_SP1.DATA<27>
312	3.312	VP1_SP1.DATA<28>
313	3.313	VP1_SP1.DATA<34>
314	3.314	VP1_SP1.DATA<35>
315	3.315	VP1_SP1.DATA<36>
316	3.316	VP1_SP1.DATA<42>
317	3.317	VP1_SP1.DATA<43>
318	3.318	VP1_SP1.DATA<44>
319	3.319	VP1_SP1.DATA<50>
320	3.320	VP1_SP1.DATA<51>
321	3.321	VP1_SP1.DATA<52>
322	3.322	VP1_SP1.DATA<56>
323	3.323	VP1_SP1.DATA<59>
324	3.324	VP1_SP1.DATA<60>
325	3.325	
326	3.326	
327	3.327	
328	3.328	
329	3.329	
330	3.330	
331	3.331	
332	3.332	
333	3.333	
334	3.334	
335	3.335	
336	3.336	
337	3.337	
338	3.338	
339	3.339	
340	3.340	

401	3.401	SP1_VP1.DATA<2>
402	3.402	SP1_VP1.DATA<3>
403	3.403	SP1_VP1.DATA<4>
404	3.404	SP1_VP1.DATA<10>
405	3.405	SP1_VP1.DATA<11>
406	3.406	SP1_VP1.DATA<12>
407	3.407	SP1_VP1.DATA<18>
408	3.408	SP1_VP1.DATA<19>
409	3.409	SP1_VP1.DATA<20>
410	3.410	SP1_VP1.DATA<26>
411	3.411	SP1_VP1.DATA<27>
412	3.412	SP1_VP1.DATA<28>
413	3.413	SP1_VP1.DATA<34>
414	3.414	SP1_VP1.DATA<35>
415	3.415	SP1_VP1.DATA<36>
416	3.416	SP1_VP1.DATA<42>
417	3.417	SP1_VP1.DATA<43>
418	3.418	SP1_VP1.DATA<44>
419	3.419	SP1_VP1.DATA<50>
420	3.420	SP1_VP1.DATA<51>
421	3.421	SP1_VP1.DATA<52>
422	3.422	SP1_VP1.DATA<56>
423	3.423	SP1_VP1.DATA<59>
424	3.424	SP1_VP1.DATA<60>
425	3.425	
426	3.426	
427	3.427	
428	3.428	
429	3.429	
430	3.430	
431	3.431	
432	3.432	
433	3.433	
434	3.434	
435	3.435	
436	3.436	
437	3.437	
438	3.438	
439	3.439	SP1_VP1.CNTX_CTL<1>
440	3.440	SP1_VP1.CNTX_CTL<0>

501	3.501	
502	3.502	
503	3.503	
504	3.504	
505	3.505	
506	3.506	
507	3.507	
508	3.508	
509	3.509	
510	3.510	
511	3.511	
512	3.512	
513	3.513	
514	3.514	
515	3.515	
516	3.516	
517	3.517	
518	3.518	
519	3.519	
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521	3.521	
522	3.522	
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524	3.524	
525	3.525	
526	3.526	
527	3.527	
528	3.528	
529	3.529	
530	3.530	
531	3.531	
532	3.532	
533	3.533	
534	3.534	
535	3.535	
536	3.536	
537	3.537	
538	3.538	
539	3.539	
540	3.540	GND<G

SECTION 3

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TITLE: CBPR

DRAWING: 411-001207-300A REV 0.0

REVISED: Thu Aug 16 20:47:52 1990

ABBR: CBPR

ENGR: GOLEMBIESKI

PAGE: 9 of 21

8

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AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP1 36P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=4

GROUND ALL PINS ON THIS ROW!

101	4_101 SP1_XSE_CTL_PAR<4>
102	4_102 SP1_XSE_CTL_PAR<3>
103	4_103 SP1_XSE_CTL_PAR<2>
104	4_104 SP1_XSE_CTL_PAR<1>
105	4_105 SP1_XSE_CTL_PAR<0>
106	4_106 SP1_XSE_WR_ZONE<3>
107	4_107 SP1_XSE_WR_ZONE<2>
108	4_108 SP1_XSE_WR_ZONE<1>
109	4_109 SP1_XSE_WR_ZONE<0>
110	4_110
111	4_111
112	4_112
113	4_113
114	4_114
115	4_115
116	4_116
117	4_117 SP1_VPI_SPARE3
118	4_118 SP1_VPI_SPARE2
119	4_119 SP1_VPI_SPARE1
120	4_120 SP1_VPI_SPARE0
121	4_121
122	4_122
123	4_123 VP1_SP1_UXA_ADDR_PAR<3>
124	4_124 VP1_SP1_UXA_ADDR<0>
125	4_125 VP1_SP1_UXA_ADDR<1>
126	4_126 VP1_SP1_UXA_ADDR<2>
127	4_127 VP1_SP1_UXA_ADDR<3>
128	4_128 VP1_SP1_UXA_ADDR<4>
129	4_129 VP1_SP1_UXA_ADDR<5>
130	4_130 VP1_SP1_UXA_ADDR<6>
131	4_131 VP1_SP1_UXA_ADDR<7>
132	4_132 VP1_SP1_UXA_ADDR_PAR<2>
133	4_133 VP1_SP1_UXA_ADDR<8>
134	4_134 VP1_SP1_UXA_ADDR<9>
135	4_135 VP1_SP1_UXA_ADDR<10>
136	4_136 VP1_SP1_UXA_ADDR<11>
137	4_137 VP1_SP1_UXA_ADDR<12>
138	4_138 VP1_SP1_UXA_ADDR<13>
139	4_139 VP1_SP1_UXA_ADDR<14>
140	4_140 VP1_SP1_UXA_ADDR<15>

201	4_201 SP1_XSE_CYCLE<0>
202	4_202 SP1_XSE_CYCLE<1>
203	4_203 SP1_XSE_BD_SEL<0>
204	4_204 SP1_XSE_BD_SEL<1>
205	4_205 SP1_XSE_BD_SEL<2>
206	4_206 SP1_XSE_BD_SEL<3>
207	4_207 SP1_XSE_ADDR<3>
208	4_208 SP1_XSE_ADDR<4>
209	4_209 SP1_XSE_ADDR<5>
210	4_210 SP1_XSE_ADDR<6>
211	4_211 SP1_XSE_ADDR<7>
212	4_212 SP1_XSE_ADDR<8>
213	4_213 SP1_XSE_ADDR<9>
214	4_214 SP1_XSE_ADDR<10>
215	4_215 SP1_XSE_ADDR<11>
216	4_216 SP1_XSE_ADDR<12>
217	4_217 SP1_XSE_ADDR<13>
218	4_218 SP1_XSE_ADDR<14>
219	4_219 SP1_XSE_ADDR<15>
220	4_220 SP1_XSE_ADDR<16>
221	4_221 SP1_XSE_ADDR<17>
222	4_222 SP1_XSE_ADDR<18>
223	4_223 SP1_XSE_ADDR<19>
224	4_224 SP1_XSE_ADDR<20>
225	4_225 SP1_XSE_ADDR<21>
226	4_226 SP1_XSE_ADDR<22>
227	4_227 SP1_XSE_ADDR<23>
228	4_228 SP1_XSE_ADDR<24>
229	4_229 SP1_XSE_ADDR<25>
230	4_230 SP1_XSE_ADDR<26>
231	4_231 SP1_XSE_ADDR<27>
232	4_232 SP1_XSE_ADDR<28>
233	4_233
234	4_234
235	4_235
236	4_236
237	4_237
238	4_238
239	4_239
240	4_240

301	4_301 SP1_XSO_CTL_PAR<4>
302	4_302 SP1_XSO_CTL_PAR<3>
303	4_303 SP1_XSO_CTL_PAR<2>
304	4_304 SP1_XSO_CTL_PAR<1>
305	4_305 SP1_XSO_CTL_PAR<0>
306	4_306 SP1_XSO_WR_ZONE<3>
307	4_307 SP1_XSO_WR_ZONE<2>
308	4_308 SP1_XSO_WR_ZONE<1>
309	4_309 SP1_XSO_WR_ZONE<0>
310	4_310
311	4_311
312	4_312
313	4_313
314	4_314
315	4_315
316	4_316
317	4_317
318	4_318
319	4_319
320	4_320
321	4_321
322	4_322
323	4_323
324	4_324
325	4_325 XC_SP1_TRAP_VECT<0>
326	4_326 XC_SP1_TRAP_VECT<1>
327	4_327 XC_SP1_TRAP_VECT<2>
328	4_328 XC_SP1_TRAP_VECT<3>
329	4_329 XC_SP1_TRAP_TYPE<0>
330	4_330 XC_SP1_TRAP_TYPE<1>
331	4_331 XC_SP1_TRAP_TYPE<2>
332	4_332 XC_SP1_TRAP_TYPE<3>
333	4_333 XC_SP1_TRAP_VECT<4>
334	4_334 XC_SP1_TRAP_VECT<5>
335	4_335 XC_SP1_TRAP_VECT<6>
336	4_336 XC_SP1_TRAP_VECT<7>
337	4_337 XC_SP1_TRAP_VECT<8>
338	4_338 XC_SP1_TRAP_VECT<9>
339	4_339 XC_SP1_TRAP_VECT<10>
340	4_340 XC_SP1_TRAP_VECT<11>

401	4_401 SP1_XSO_CYCLE<0>
402	4_402 SP1_XSO_CYCLE<1>
403	4_403 SP1_XSO_BD_SEL<0>
404	4_404 SP1_XSO_BD_SEL<1>
405	4_405 SP1_XSO_BD_SEL<2>
406	4_406 SP1_XSO_BD_SEL<3>
407	4_407 SP1_XSO_ADDR<3>
408	4_408 SP1_XSO_ADDR<4>
409	4_409 SP1_XSO_ADDR<5>
410	4_410 SP1_XSO_ADDR<6>
411	4_411 SP1_XSO_ADDR<7>
412	4_412 SP1_XSO_ADDR<8>
413	4_413 SP1_XSO_ADDR<9>
414	4_414 SP1_XSO_ADDR<10>
415	4_415 SP1_XSO_ADDR<11>
416	4_416 SP1_XSO_ADDR<12>
417	4_417 SP1_XSO_ADDR<13>
418	4_418 SP1_XSO_ADDR<14>
419	4_419 SP1_XSO_ADDR<15>
420	4_420 SP1_XSO_ADDR<16>
421	4_421 SP1_XSO_ADDR<17>
422	4_422 SP1_XSO_ADDR<18>
423	4_423 SP1_XSO_ADDR<19>
424	4_424 SP1_XSO_ADDR<20>
425	4_425 SP1_XSO_ADDR<21>
426	4_426 SP1_XSO_ADDR<22>
427	4_427 SP1_XSO_ADDR<23>
428	4_428 SP1_XSO_ADDR<24>
429	4_429 SP1_XSO_ADDR<25>
430	4_430 SP1_XSO_ADDR<26>
431	4_431 SP1_XSO_ADDR<27>
432	4_432 SP1_XSO_ADDR<28>
433	4_433
434	4_434
435	4_435
436	4_436
437	4_437
438	4_438
439	4_439
440	4_440

501	4_501
502	4_502
503	4_503
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528	4_528
529	4_529
530	4_530
531	4_531
532	4_532
533	4_533
534	4_534
535	4_535
536	4_536
537	4_537
538	4_538
539	4_539
540	4_540 GND/G

SECTION 4

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 REVISED: Thu Aug 16 20:48:43 1990

ABBR: CBPR
 ENGR: GOLEMBIESKI

PAGE: 10 of 21

8

7

6

3

2

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AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP1 109P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=5

GROUND ALL PINS ON THIS ROW!

101	5_101 XC_SP1.SCAN_CTL<2>
102	5_102 XC_SP1.SCAN_IN
103	5_103 XRE_SP1.RD_RDY
104	5_104 XRO_SP1.RD_RDY
105	5_105 XSO_SP1.A_REQ_NEXT
106	5_106 XSO_SP1.A_REQ_PEND
107	5_107 XSO_SP1.A_ST_PEND
108	5_108 XSO_SP1.B_REQ_NEXT
109	5_109 XSO_SP1.B_REQ_PEND
110	5_110 XSO_SP1.B_ST_HUNG
111	5_111 XSE_SP1.A_REQ_NEXT
112	5_112 XSE_SP1.A_REQ_PEND
113	5_113 XSE_SP1.A_ST_PEND
114	5_114 XSE_SP1.B_REQ_NEXT
115	5_115 XSE_SP1.B_REQ_PEND
116	5_116 XSE_SP1.B_ST_PEND
117	5_117 XRO_SP1.RD_PAR<3>
118	5_118 XRO_SP1.RD_DATA<0>
119	5_119 XRO_SP1.RD_DATA<1>
120	5_120 XRO_SP1.RD_PAR<2>
121	5_121 XRO_SP1.RD_DATA<8>
122	5_122 XRO_SP1.RD_DATA<9>
123	5_123 XRO_SP1.RD_PAR<1>
124	5_124 XRO_SP1.RD_DATA<16>
125	5_125 XRO_SP1.RD_DATA<17>
126	5_126 XRO_SP1.RD_PAR<0>
127	5_127 XRO_SP1.RD_DATA<24>
128	5_128 XRO_SP1.RD_DATA<25>
129	5_129 XRE_SP1.RD_PAR<3>
130	5_130 XRE_SP1.RD_DATA<0>
131	5_131 XRE_SP1.RD_DATA<1>
132	5_132 XRE_SP1.RD_PAR<2>
133	5_133 XRE_SP1.RD_DATA<8>
134	5_134 XRE_SP1.RD_DATA<9>
135	5_135 XRE_SP1.RD_PAR<1>
136	5_136 XRE_SP1.RD_DATA<16>
137	5_137 XRE_SP1.RD_DATA<17>
138	5_138 XRE_SP1.RD_PAR<0>
139	5_139 XRE_SP1.RD_DATA<24>
140	5_140 XRE_SP1.RD_DATA<25>

201	5_201 XC_SP1.SCAN_CTL<1>
202	5_202 SP1_XC.SCAN_OUT
203	5_203 SP1_XSE.RDY
204	5_204 SP1_XSO.RDY
205	5_205 SP1_XRE.RTN_PAR_ERR
206	5_206 SP1_XRO.RTN_PAR_ERR
207	5_207
208	5_208 SP1_XC.DEADLOCK
209	5_209 SP1_XC.TRAP_COMP
210	5_210 SP1_XC.HW_HUNG
211	5_211 XC_SP1.TRAP_RDY
212	5_212 XC_SP1.MT_COMP
213	5_213 XC_SP1.CU_STATUS_EN
214	5_214 XC_SP1.CU_STATUS
215	5_215 XC_SP1.USEC_EN
216	5_216
217	5_217 SP1_XSO.WR_PAR<3>
218	5_218 SP1_XSO.WR_DATA<0>
219	5_219 SP1_XSO.WR_DATA<1>
220	5_220 SP1_XSO.WR_PAR<2>
221	5_221 SP1_XSO.WR_DATA<8>
222	5_222 SP1_XSO.WR_DATA<9>
223	5_223 SP1_XSO.WR_PAR<1>
224	5_224 SP1_XSO.WR_DATA<16>
225	5_225 SP1_XSO.WR_DATA<17>
226	5_226 SP1_XSO.WR_PAR<0>
227	5_227 SP1_XSO.WR_DATA<24>
228	5_228 SP1_XSO.WR_DATA<25>
229	5_229 SP1_XSE.WR_PAR<3>
230	5_230 SP1_XSE.WR_DATA<0>
231	5_231 SP1_XSE.WR_DATA<1>
232	5_232 SP1_XSE.WR_PAR<2>
233	5_233 SP1_XSE.WR_DATA<8>
234	5_234 SP1_XSE.WR_DATA<9>
235	5_235 SP1_XSE.WR_PAR<1>
236	5_236 SP1_XSE.WR_DATA<16>
237	5_237 SP1_XSE.WR_DATA<17>
238	5_238 SP1_XSE.WR_PAR<0>
239	5_239 SP1_XSE.WR_DATA<24>
240	5_240 SP1_XSE.WR_DATA<25>

301	5_301 XC_SP1.SCAN_CTL<0>
302	5_302 VP1_SP1.DISP_REQ_NEXT
303	5_303
304	5_304 VP1_SP1.UXM_RDY
305	5_305 VP1_SP1.UXS_RDY
306	5_306 VP1_SP1.UXA_UK<0>
307	5_307 VP1_SP1.UXA_UK<1>
308	5_308 VP1_SP1.UXA_LAST
309	5_309 SP1_XS0E.SPARE1
310	5_310 SP1_XS1E.SPARE0
311	5_311 SP1_XS1E.SPARE1
312	5_312 SP1_XS1E.SPARE0
313	5_313 XRE_SP1.SPARE1
314	5_314 XRE_SP1.SPARE0
315	5_315 SP1_XC.SOFT_ERROR
316	5_316 XC_SP1.SLOG_ENA
317	5_317 VP1_SP1.PAR<7>
318	5_318 VP1_SP1.DATA<0>
319	5_319 VP1_SP1.DATA<1>
320	5_320 VP1_SP1.PAR<6>
321	5_321 VP1_SP1.DATA<8>
322	5_322 VP1_SP1.DATA<9>
323	5_323 VP1_SP1.PAR<5>
324	5_324 VP1_SP1.DATA<16>
325	5_325 VP1_SP1.DATA<17>
326	5_326 VP1_SP1.PAR<4>
327	5_327 VP1_SP1.DATA<24>
328	5_328 VP1_SP1.DATA<25>
329	5_329 VP1_SP1.PAR<3>
330	5_330 VP1_SP1.DATA<32>
331	5_331 VP1_SP1.DATA<33>
332	5_332 VP1_SP1.PAR<2>
333	5_333 VP1_SP1.DATA<40>
334	5_334 VP1_SP1.DATA<41>
335	5_335 VP1_SP1.PAR<1>
336	5_336 VP1_SP1.DATA<48>
337	5_337 VP1_SP1.DATA<49>
338	5_338 VP1_SP1.PAR<0>
339	5_339 VP1_SP1.DATA<56>
340	5_340 VP1_SP1.DATA<57>

401	5_401 SP1_XC.HARD_ERROR
402	5_402 SP1_VP1.SXV_RDY
403	5_403 SP1_VP1.UX_REQ_NEXT
404	5_404 SP1_VP1.MXV_RDY
405	5_405 SP1_XS00.SPARE1
406	5_406 SP1_XS00.SPARE0
407	5_407 SP1_XS10.SPARE1
408	5_408 SP1_XS10.SPARE0
409	5_409 XRO_SP1.SPARE1
410	5_410 XRO_SP1.SPARE0
411	5_411
412	5_412 SP1_XC.STOP_CNTR
413	5_413 XC_SP1.SPARE2
414	5_414 XC_SP1.SPARE1
415	5_415 XC_SP1.SPARE0
416	5_416
417	5_417 SP1_VP1.PAR<7>
418	5_418 SP1_VP1.DATA<0>
419	5_419 SP1_VP1.DATA<1>
420	5_420 SP1_VP1.PAR<6>
421	5_421 SP1_VP1.DATA<8>
422	5_422 SP1_VP1.DATA<9>
423	5_423 SP1_VP1.PAR<5>
424	5_424 SP1_VP1.DATA<16>
425	5_425 SP1_VP1.DATA<17>
426	5_426 SP1_VP1.PAR<4>
427	5_427 SP1_VP1.DATA<24>
428	5_428 SP1_VP1.DATA<25>
429	5_429 SP1_VP1.PAR<3>
430	5_430 SP1_VP1.DATA<32>
431	5_431 SP1_VP1.DATA<33>
432	5_432 SP1_VP1.PAR<2>
433	5_433 SP1_VP1.DATA<40>
434	5_434 SP1_VP1.DATA<41>
435	5_435 SP1_VP1.PAR<1>
436	5_436 SP1_VP1.DATA<48>
437	5_437 SP1_VP1.DATA<49>
438	5_438 SP1_VP1.PAR<0>
439	5_439 SP1_VP1.DATA<56>
440	5_440 SP1_VP1.DATA<57>

501	5_501
502	5_502
503	5_503
504	5_504
505	5_505
506	5_506
507	5_507
508	5_508
509	5_509
510	5_510
511	5_511
512	5_512
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514	5_514
515	5_515
516	5_516
517	5_517
518	5_518
519	5_519
520	5_520
521	5_521
522	5_522
523	5_523
524	5_524
525	5_525
526	5_526
527	5_527
528	5_528
529	5_529
530	5_530
531	5_531
532	5_532
533	5_533
534	5_534
535	5_535
536	5_536
537	5_537
538	5_538
539	5_539
540	5_540 GND\G

SECTION 5 (TOP)

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 DRAWING: 411-001207-300A REV 0.0
 REVISION: Fri Aug 17 09:26:31 1990
 PAGE: 11 of 21
 ABBR: CBPR
 ENGR: GOLENBIESKI

8

7

6

5

4

3

2

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AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP1 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=1

GROUND ALL PINS ON THIS ROW!

101	1-101
102	1-102
103	1-103
104	1-104
105	1-105
106	1-106
107	1-107
108	1-108
109	1-109
110	1-110
111	1-111
112	1-112
113	1-113
114	1-114
115	1-115
116	1-116
117	1-117
118	1-118
119	1-119
120	1-120
121	1-121
122	1-122
123	1-123
124	1-124
125	1-125
126	1-126
127	1-127
128	1-128
129	1-129
130	1-130
131	1-131
132	1-132
133	1-133
134	1-134
135	1-135
136	1-136 BP_VP1.PORTID<3>
137	1-137 VP1_BP.LED.INTL.OUT
138	1-138 BP_VP1.BPTYPE<3>
139	1-139 BP_VP1.SLOTID<3>
140	1-140 CU_VP1.CLOCK_3X

201	1-201
202	1-202
203	1-203
204	1-204
205	1-205
206	1-206
207	1-207
208	1-208
209	1-209
210	1-210
211	1-211
212	1-212
213	1-213
214	1-214
215	1-215
216	1-216
217	1-217
218	1-218
219	1-219
220	1-220
221	1-221
222	1-222
223	1-223
224	1-224
225	1-225
226	1-226
227	1-227
228	1-228
229	1-229
230	1-230
231	1-231
232	1-232
233	1-233
234	1-234
235	1-235
236	1-236 BP_VP1.PORTID<2>
237	1-237 BP_VP1.LED.INTL.IN
238	1-238 BP_VP1.BPTYPE<2>
239	1-239 BP_VP1.SLOTID<2>
240	1-240 CU_VP1.CLOCK_3X*

301	1-301	VP1-SP1.IDLE
302	1-302	
303	1-303	
304	1-304	
305	1-305	
306	1-306	
307	1-307	
308	1-308	
309	1-309	
310	1-310	
311	1-311	
312	1-312	
313	1-313	
314	1-314	
315	1-315	
316	1-316	
317	1-317	
318	1-318	
319	1-319	
320	1-320	
321	1-321	
322	1-322	
323	1-323	
324	1-324	
325	1-325	
326	1-326	
327	1-327	
328	1-328	
329	1-329	
330	1-330	
331	1-331	
332	1-332	
333	1-333	
334	1-334	
335	1-335	
336	1-336	
337	1-337	BP_VP1.PORTID<1>
338	1-338	BP_VP1.BPTYPE<1>
339	1-339	BP_VP1.SLOTID<1>
340	1-340	

401	1-401	SP1_VP1.DISP_EP<10>
402	1-402	SP1_VP1.DISP_EP<9>
403	1-403	SP1_VP1.DISP_EP<8>
404	1-404	SP1_VP1.DISP_EP<7>
405	1-405	SP1_VP1.DISP_EP<6>
406	1-406	SP1_VP1.DISP_EP<5>
407	1-407	SP1_VP1.DISP_EP<4>
408	1-408	SP1_VP1.DISP_EP<3>
409	1-409	SP1_VP1.DISP_EP<2>
410	1-410	SP1_VP1.DISP_EP<1>
411	1-411	SP1_VP1.DISP_EP<0>
412	1-412	SP1_VP1.DISP_IREG<2>
413	1-413	SP1_VP1.DISP_IREG<1>
414	1-414	SP1_VP1.DISP_IREG<0>
415	1-415	SP1_VP1.DISP_JREG<2>
416	1-416	SP1_VP1.DISP_JREG<1>
417	1-417	SP1_VP1.DISP_JREG<0>
418	1-418	SP1_VP1.DISP_KREG<2>
419	1-419	SP1_VP1.DISP_KREG<1>
420	1-420	SP1_VP1.DISP_KREG<0>
421	1-421	
422	1-422	SP1_VP1.IEEE
423	1-423	
424	1-424	
425	1-425	
426	1-426	
427	1-427	
428	1-428	
429	1-429	
430	1-430	
431	1-431	
432	1-432	
433	1-433	
434	1-434	
435	1-435	
436	1-436	
437	1-437	BP_VP1.PORTID<0>
438	1-438	BP_VP1.BPTYPE<0>
439	1-439	BP_VP1.SLOTID<0>
440	1-440	

501	1-501
502	1-502
503	1-503
504	1-504
505	1-505
506	1-506
507	1-507
508	1-508
509	1-509
510	1-510
511	1-511
512	1-512
513	1-513
514	1-514
515	1-515
516	1-516
517	1-517
518	1-518
519	1-519
520	1-520
521	1-521
522	1-522
523	1-523
524	1-524
525	1-525
526	1-526
527	1-527
528	1-528
529	1-529
530	1-530
531	1-531
532	1-532
533	1-533
534	1-534
535	1-535
536	1-536
537	1-537
538	1-538
539	1-539
540	1-540

GND\G

CONNECTOR 1 (BOTTOM)

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TITLE: CBPR
 DRAWING: 411-001207-300A REV 0.0
 REVISED: Thu Aug 16 20:50:30 1990

ABBR: CBPR
 ENGR: GOLENBIESKI

PAGE: 12 of 21

8

7

6

3

2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP1 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=2

GROUND ALL PINS ON THIS ROW!

101	2_101
102	2_102
103	2_103
104	2_104
105	2_105
106	2_105
107	2_107
108	2_108
109	2_109
110	2_110
111	2_111
112	2_112
113	2_113
114	2_114
115	2_115
116	2_116
117	2_117
118	2_118
119	2_119
120	2_120
121	2_121
122	2_122
123	2_123
124	2_124
125	2_125
126	2_126
127	2_127
128	2_128
129	2_129
130	2_130
131	2_131
132	2_132
133	2_133
134	2_134
135	2_135
136	2_136
137	2_137 VP1_SPI.SPARE3
138	2_138 VP1_SPI.SPARE2
139	2_139 VP1_SPI.SPARE1
140	2_140 VP1_SPI.SPARE0

201	2_201
202	2_202
203	2_203
204	2_204
205	2_205
206	2_206
207	2_207
208	2_208
209	2_209
210	2_210
211	2_211
212	2_212
213	2_213
214	2_214
215	2_215
216	2_216
217	2_217
218	2_218
219	2_219
220	2_220
221	2_221
222	2_222
223	2_223
224	2_224
225	2_225
226	2_226
227	2_227
228	2_228
229	2_229
230	2_230
231	2_231
232	2_232
233	2_233
234	2_234
235	2_235
236	2_236
237	2_237
238	2_238
239	2_239
240	2_240

301	2_301	VP1_SPI.DATA<5>
302	2_302	VP1_SPI.DATA<6>
303	2_303	VP1_SPI.DATA<7>
304	2_304	VP1_SPI.DATA<13>
305	2_305	VP1_SPI.DATA<14>
306	2_306	VP1_SPI.DATA<15>
307	2_307	VP1_SPI.DATA<21>
308	2_308	VP1_SPI.DATA<22>
309	2_309	VP1_SPI.DATA<23>
310	2_310	VP1_SPI.DATA<29>
311	2_311	VP1_SPI.DATA<30>
312	2_312	VP1_SPI.DATA<31>
313	2_313	VP1_SPI.DATA<37>
314	2_314	VP1_SPI.DATA<38>
315	2_315	VP1_SPI.DATA<39>
316	2_316	VP1_SPI.DATA<45>
317	2_317	VP1_SPI.DATA<46>
318	2_318	VP1_SPI.DATA<47>
319	2_319	VP1_SPI.DATA<53>
320	2_320	VP1_SPI.DATA<54>
321	2_321	VP1_SPI.DATA<55>
322	2_322	VP1_SPI.DATA<61>
323	2_323	VP1_SPI.DATA<62>
324	2_324	VP1_SPI.DATA<63>
325	2_325	
326	2_326	
327	2_327	
328	2_328	
329	2_329	
330	2_330	VP1_SPI.MXV_REQ_NEXT
331	2_331	VP1_SPI.SXV_REQ_NEXT
332	2_332	
333	2_333	VP1_SPI.PSW_HAZ
334	2_334	VP1_SPI.SET_FDZ
335	2_335	VP1_SPI.SET_FSN
336	2_336	VP1_SPI.SET_OV
337	2_337	VP1_SPI.SET_RO
338	2_338	VP1_SPI.SET_SDZ
339	2_339	VP1_SPI.SET_SIU
340	2_340	VP1_SPI.SET_UN

401	2_401	SP1_VP1.DATA<5>
402	2_402	SP1_VP1.DATA<6>
403	2_403	SP1_VP1.DATA<7>
404	2_404	SP1_VP1.DATA<13>
405	2_405	SP1_VP1.DATA<14>
406	2_406	SP1_VP1.DATA<15>
407	2_407	SP1_VP1.DATA<21>
408	2_408	SP1_VP1.DATA<22>
409	2_409	SP1_VP1.DATA<23>
410	2_410	SP1_VP1.DATA<29>
411	2_411	SP1_VP1.DATA<30>
412	2_412	SP1_VP1.DATA<31>
413	2_413	SP1_VP1.DATA<37>
414	2_414	SP1_VP1.DATA<38>
415	2_415	SP1_VP1.DATA<39>
416	2_416	SP1_VP1.DATA<45>
417	2_417	SP1_VP1.DATA<46>
418	2_418	SP1_VP1.DATA<47>
419	2_419	SP1_VP1.DATA<53>
420	2_420	SP1_VP1.DATA<54>
421	2_421	SP1_VP1.DATA<55>
422	2_422	SP1_VP1.DATA<61>
423	2_423	SP1_VP1.DATA<62>
424	2_424	SP1_VP1.DATA<63>
425	2_425	
426	2_426	
427	2_427	
428	2_428	
429	2_429	
430	2_430	
431	2_431	
432	2_432	SP1_VP1.DISP_RDY
433	2_433	SP1_VP1.DISP_PSW_HAZ
434	2_434	
435	2_435	
436	2_436	
437	2_437	
438	2_438	
439	2_439	
440	2_440	

501	2_501
502	2_502
503	2_503
504	2_504
505	2_505
506	2_506
507	2_507
508	2_508
509	2_509
510	2_510
511	2_511
512	2_512
513	2_513
514	2_514
515	2_515
516	2_516
517	2_517
518	2_518
519	2_519
520	2_520
521	2_521
522	2_522
523	2_523
524	2_524
525	2_525
526	2_526
527	2_527
528	2_528
529	2_529
530	2_530
531	2_531
532	2_532
533	2_533
534	2_534
535	2_535
536	2_536
537	2_537
538	2_538
539	2_539
540	2_540 GND\G

CONNECTOR 2

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TITLE: CBPR
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 REVISED: Thu Aug 16 20:51:19 1990

ABBR: CBPR
 ENGR: GOLENBIESKI

PAGE: 13 of 21

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP1 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=3

GROUND ALL PINS ON THIS ROW!

101	3_101	
102	3_102	
103	3_103	
104	3_104	
105	3_105	
106	3_106	
107	3_107	
108	3_108	
109	3_109	
110	3_110	
111	3_111	
112	3_112	
113	3_113	
114	3_114	
115	3_115	
116	3_116	
117	3_117	
118	3_118	
119	3_119	
120	3_120	
121	3_121	
122	3_122	
123	3_123	
124	3_124	
125	3_125	
126	3_126	
127	3_127	
128	3_128	
129	3_129	
130	3_130	
131	3_131	
132	3_132	VP1_SP1.VXA_ADDR<0>
133	3_133	VP1_SP1.VXA_ADDR<24>
134	3_134	VP1_SP1.VXA_ADDR<25>
135	3_135	VP1_SP1.VXA_ADDR<26>
136	3_136	VP1_SP1.VXA_ADDR<27>
137	3_137	VP1_SP1.VXA_ADDR<28>
138	3_138	VP1_SP1.VXA_ADDR<29>
139	3_139	VP1_SP1.VXA_ADDR<30>
140	3_140	VP1_SP1.VXA_ADDR<31>

201	3_201	
202	3_202	
203	3_203	
204	3_204	
205	3_205	
206	3_206	
207	3_207	
208	3_208	
209	3_209	
210	3_210	
211	3_211	
212	3_212	
213	3_213	
214	3_214	
215	3_215	
216	3_216	
217	3_217	
218	3_218	
219	3_219	
220	3_220	
221	3_221	
222	3_222	
223	3_223	
224	3_224	
225	3_225	
226	3_226	
227	3_227	
228	3_228	
229	3_229	
230	3_230	
231	3_231	
232	3_232	VP1_SP1.VXA_ADDR<1>
233	3_233	VP1_SP1.VXA_ADDR<16>
234	3_234	VP1_SP1.VXA_ADDR<17>
235	3_235	VP1_SP1.VXA_ADDR<18>
236	3_236	VP1_SP1.VXA_ADDR<19>
237	3_237	VP1_SP1.VXA_ADDR<20>
238	3_238	VP1_SP1.VXA_ADDR<21>
239	3_239	VP1_SP1.VXA_ADDR<22>
240	3_240	VP1_SP1.VXA_ADDR<23>

301	3_301	VP1_SP1.DATA<2>
302	3_302	VP1_SP1.DATA<3>
303	3_303	VP1_SP1.DATA<4>
304	3_304	VP1_SP1.DATA<10>
305	3_305	VP1_SP1.DATA<11>
306	3_306	VP1_SP1.DATA<12>
307	3_307	VP1_SP1.DATA<18>
308	3_308	VP1_SP1.DATA<19>
309	3_309	VP1_SP1.DATA<20>
310	3_310	VP1_SP1.DATA<26>
311	3_311	VP1_SP1.DATA<27>
312	3_312	VP1_SP1.DATA<28>
313	3_313	VP1_SP1.DATA<34>
314	3_314	VP1_SP1.DATA<35>
315	3_315	VP1_SP1.DATA<36>
316	3_316	VP1_SP1.DATA<42>
317	3_317	VP1_SP1.DATA<43>
318	3_318	VP1_SP1.DATA<44>
319	3_319	VP1_SP1.DATA<50>
320	3_320	VP1_SP1.DATA<51>
321	3_321	VP1_SP1.DATA<52>
322	3_322	VP1_SP1.DATA<58>
323	3_323	VP1_SP1.DATA<59>
324	3_324	VP1_SP1.DATA<60>
325	3_325	
326	3_326	
327	3_327	
328	3_328	
329	3_329	
330	3_330	
331	3_331	
332	3_332	
333	3_333	
334	3_334	
335	3_335	
336	3_336	
337	3_337	
338	3_338	
339	3_339	
340	3_340	

401	3_401	SP1_VP1.DATA<2>
402	3_402	SP1_VP1.DATA<3>
403	3_403	SP1_VP1.DATA<4>
404	3_404	SP1_VP1.DATA<10>
405	3_405	SP1_VP1.DATA<11>
406	3_406	SP1_VP1.DATA<12>
407	3_407	SP1_VP1.DATA<18>
408	3_408	SP1_VP1.DATA<19>
409	3_409	SP1_VP1.DATA<20>
410	3_410	SP1_VP1.DATA<26>
411	3_411	SP1_VP1.DATA<27>
412	3_412	SP1_VP1.DATA<28>
413	3_413	SP1_VP1.DATA<34>
414	3_414	SP1_VP1.DATA<35>
415	3_415	SP1_VP1.DATA<36>
416	3_416	SP1_VP1.DATA<42>
417	3_417	SP1_VP1.DATA<43>
418	3_418	SP1_VP1.DATA<44>
419	3_419	SP1_VP1.DATA<50>
420	3_420	SP1_VP1.DATA<51>
421	3_421	SP1_VP1.DATA<52>
422	3_422	SP1_VP1.DATA<58>
423	3_423	SP1_VP1.DATA<59>
424	3_424	SP1_VP1.DATA<60>
425	3_425	
426	3_426	
427	3_427	
428	3_428	
429	3_429	
430	3_430	
431	3_431	
432	3_432	
433	3_433	
434	3_434	
435	3_435	
436	3_436	
437	3_437	
438	3_438	
439	3_439	SP1_VP1.CNTX_CTL<1>
440	3_440	SP1_VP1.CNTX_CTL<0>

501	3_501	
502	3_502	
503	3_503	
504	3_504	
505	3_505	
506	3_506	
507	3_507	
508	3_508	
509	3_509	
510	3_510	
511	3_511	
512	3_512	
513	3_513	
514	3_514	
515	3_515	
516	3_516	
517	3_517	
518	3_518	
519	3_519	
520	3_520	
521	3_521	
522	3_522	
523	3_523	
524	3_524	
525	3_525	
526	3_526	
527	3_527	
528	3_528	
529	3_529	
530	3_530	
531	3_531	
532	3_532	
533	3_533	
534	3_534	
535	3_535	
536	3_536	
537	3_537	
538	3_538	
539	3_539	
540	3_540	GND\G

CONNECTOR 3

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TITLE: CBPR
 DRAWING: 411-001207-300A REV 0.0
 REVISED: Thu Aug 16 20:52:12 1990

ABBR: CBPR
 ENGR: GOLENBIESKI

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP1 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE 'GED' SECTION COMMAND WILL NOT WORK.
 SEC=4

GROUND ALL PINS ON THIS ROW!

101	4_101	
102	4_102	
103	4_103	
104	4_104	
105	4_105	
106	4_106	
107	4_107	
108	4_108	
109	4_109	
110	4_110	
111	4_111	
112	4_112	
113	4_113	
114	4_114	
115	4_115	
116	4_116	
117	4_117	SPI_VP1_SPARE3
118	4_118	SPI_VP1_SPARE2
119	4_119	SPI_VP1_SPARE1
120	4_120	SPI_VP1_SPARE0
121	4_121	
122	4_122	
123	4_123	VP1_SPI_UXA_ADDR_PAR<3>
124	4_124	VP1_SPI_UXA_ADDR<0>
125	4_125	VP1_SPI_UXA_ADDR<1>
126	4_126	VP1_SPI_UXA_ADDR<2>
127	4_127	VP1_SPI_UXA_ADDR<3>
128	4_128	VP1_SPI_UXA_ADDR<4>
129	4_129	VP1_SPI_UXA_ADDR<5>
130	4_130	VP1_SPI_UXA_ADDR<6>
131	4_131	VP1_SPI_UXA_ADDR<7>
132	4_132	VP1_SPI_UXA_ADDR_PAR<2>
133	4_133	VP1_SPI_UXA_ADDR<8>
134	4_134	VP1_SPI_UXA_ADDR<9>
135	4_135	VP1_SPI_UXA_ADDR<10>
136	4_136	VP1_SPI_UXA_ADDR<11>
137	4_137	VP1_SPI_UXA_ADDR<12>
138	4_138	VP1_SPI_UXA_ADDR<13>
139	4_139	VP1_SPI_UXA_ADDR<14>
140	4_140	VP1_SPI_UXA_ADDR<15>

201	4_201
202	4_202
203	4_203
204	4_204
205	4_205
206	4_206
207	4_207
208	4_208
209	4_209
210	4_210
211	4_211
212	4_212
213	4_213
214	4_214
215	4_215
216	4_216
217	4_217
218	4_218
219	4_219
220	4_220
221	4_221
222	4_222
223	4_223
224	4_224
225	4_225
226	4_226
227	4_227
228	4_228
229	4_229
230	4_230
231	4_231
232	4_232
233	4_233
234	4_234
235	4_235
236	4_236
237	4_237
238	4_238
239	4_239
240	4_240

301	4_301
302	4_302
303	4_303
304	4_304
305	4_305
306	4_306
307	4_307
308	4_308
309	4_309
310	4_310
311	4_311
312	4_312
313	4_313
314	4_314
315	4_315
316	4_316
317	4_317
318	4_318
319	4_319
320	4_320
321	4_321
322	4_322
323	4_323
324	4_324
325	4_325
326	4_326
327	4_327
328	4_328
329	4_329
330	4_330
331	4_331
332	4_332
333	4_333
334	4_334
335	4_335
336	4_336
337	4_337
338	4_338
339	4_339
340	4_340

401	4_401
402	4_402
403	4_403
404	4_404
405	4_405
406	4_406
407	4_407
408	4_408
409	4_409
410	4_410
411	4_411
412	4_412
413	4_413
414	4_414
415	4_415
416	4_416
417	4_417
418	4_418
419	4_419
420	4_420
421	4_421
422	4_422
423	4_423
424	4_424
425	4_425
426	4_426
427	4_427
428	4_428
429	4_429
430	4_430
431	4_431
432	4_432
433	4_433
434	4_434
435	4_435
436	4_436
437	4_437
438	4_438
439	4_439
440	4_440

501	4_501
502	4_502
503	4_503
504	4_504
505	4_505
506	4_506
507	4_507
508	4_508
509	4_509
510	4_510
511	4_511
512	4_512
513	4_513
514	4_514
515	4_515
516	4_516
517	4_517
518	4_518
519	4_519
520	4_520
521	4_521
522	4_522
523	4_523
524	4_524
525	4_525
526	4_526
527	4_527
528	4_528
529	4_529
530	4_530
531	4_531
532	4_532
533	4_533
534	4_534
535	4_535
536	4_536
537	4_537
538	4_538
539	4_539
540	4_540

GND\G

CONNECTOR 4

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 REVISOR: Thu Aug 16 20:52:52 1990
 ABBR: CBPR
 ENGR: GOLENBIESKI
 PAGE: 15 of 21

8

7

6

5

4

3

2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP1 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=5

GROUND ALL PINS ON THIS ROW!

101	5_101	XC_UP1.SCAN_CTL<2>
102	5_102	XC_UP1.SCAN_IN
103	5_103	
104	5_104	
105	5_105	
106	5_106	
107	5_107	
108	5_108	
109	5_109	
110	5_110	
111	5_111	
112	5_112	
113	5_113	
114	5_114	
115	5_115	
116	5_116	
117	5_117	
118	5_118	
119	5_119	
120	5_120	
121	5_121	
122	5_122	
123	5_123	
124	5_124	
125	5_125	
126	5_126	
127	5_127	
128	5_128	
129	5_129	
130	5_130	
131	5_131	
132	5_132	
133	5_133	
134	5_134	
135	5_135	
136	5_136	
137	5_137	
138	5_138	
139	5_139	
140	5_140	

201	5_201	XC_UP1.SCAN_CTL<1>
202	5_202	VP1_XC.SCAN_OUT
203	5_203	
204	5_204	
205	5_205	
206	5_206	
207	5_207	
208	5_208	
209	5_209	
210	5_210	
211	5_211	
212	5_212	
213	5_213	
214	5_214	
215	5_215	
216	5_216	
217	5_217	
218	5_218	
219	5_219	
220	5_220	
221	5_221	
222	5_222	
223	5_223	
224	5_224	
225	5_225	
226	5_226	
227	5_227	
228	5_228	
229	5_229	
230	5_230	
231	5_231	
232	5_232	
233	5_233	
234	5_234	
235	5_235	
236	5_236	
237	5_237	
238	5_238	
239	5_239	
240	5_240	

301	5_301	XC_UP1.SCAN_CTL<0>
302	5_302	VP1_SPI.DISP_REQ_NEXT
303	5_303	
304	5_304	VP1_SPI.UXM_RDY
305	5_305	VP1_SPI.UXS_RDY
306	5_306	VP1_SPI.UXA_VM<0>
307	5_307	VP1_SPI.UXA_VM<1>
308	5_308	VP1_SPI.UXA_LAST
309	5_309	
310	5_310	
311	5_311	
312	5_312	
313	5_313	
314	5_314	
315	5_315	
316	5_316	
317	5_317	VP1_SPI.PAR<7>
318	5_318	VP1_SPI.DATA<0>
319	5_319	VP1_SPI.DATA<1>
320	5_320	VP1_SPI.PAR<6>
321	5_321	VP1_SPI.DATA<8>
322	5_322	VP1_SPI.DATA<9>
323	5_323	VP1_SPI.PAR<5>
324	5_324	VP1_SPI.DATA<16>
325	5_325	VP1_SPI.DATA<17>
326	5_326	VP1_SPI.PAR<4>
327	5_327	VP1_SPI.DATA<24>
328	5_328	VP1_SPI.DATA<25>
329	5_329	VP1_SPI.PAR<3>
330	5_330	VP1_SPI.DATA<32>
331	5_331	VP1_SPI.DATA<33>
332	5_332	VP1_SPI.PAR<2>
333	5_333	VP1_SPI.DATA<40>
334	5_334	VP1_SPI.DATA<41>
335	5_335	VP1_SPI.PAR<1>
336	5_336	VP1_SPI.DATA<48>
337	5_337	VP1_SPI.DATA<49>
338	5_338	VP1_SPI.PAR<0>
339	5_339	VP1_SPI.DATA<56>
340	5_340	VP1_SPI.DATA<57>

401	5_401	VP1_XC.HARD_ERROR
402	5_402	SPI_VP1.SKU_RDY
403	5_403	SPI_VP1.VK_REQ_NEXT
404	5_404	SPI_VP1.MXU_RDY
405	5_405	
406	5_406	
407	5_407	
408	5_408	
409	5_409	
410	5_410	
411	5_411	
412	5_412	
413	5_413	
414	5_414	
415	5_415	
416	5_416	
417	5_417	SPI_VP1.PAR<7>
418	5_418	SPI_VP1.DATA<0>
419	5_419	SPI_VP1.DATA<1>
420	5_420	SPI_VP1.PAR<6>
421	5_421	SPI_VP1.DATA<8>
422	5_422	SPI_VP1.DATA<9>
423	5_423	SPI_VP1.PAR<5>
424	5_424	SPI_VP1.DATA<16>
425	5_425	SPI_VP1.DATA<17>
426	5_426	SPI_VP1.PAR<4>
427	5_427	SPI_VP1.DATA<24>
428	5_428	SPI_VP1.DATA<25>
429	5_429	SPI_VP1.PAR<3>
430	5_430	SPI_VP1.DATA<32>
431	5_431	SPI_VP1.DATA<33>
432	5_432	SPI_VP1.PAR<2>
433	5_433	SPI_VP1.DATA<40>
434	5_434	SPI_VP1.DATA<41>
435	5_435	SPI_VP1.PAR<1>
436	5_436	SPI_VP1.DATA<48>
437	5_437	SPI_VP1.DATA<49>
438	5_438	SPI_VP1.PAR<0>
439	5_439	SPI_VP1.DATA<56>
440	5_440	SPI_VP1.DATA<57>

501	5_501	
502	5_502	
503	5_503	
504	5_504	
505	5_505	
506	5_506	
507	5_507	
508	5_508	
509	5_509	
510	5_510	
511	5_511	
512	5_512	
513	5_513	
514	5_514	
515	5_515	
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522	5_522	
523	5_523	
524	5_524	
525	5_525	
526	5_526	
527	5_527	
528	5_528	
529	5_529	
530	5_530	
531	5_531	
532	5_532	
533	5_533	
534	5_534	
535	5_535	
536	5_536	
537	5_537	
538	5_538	
539	5_539	
540	5_540	GND\G

CONNECTOR 5 (TOP)

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TITLE: CBPR

DRAWING: 411-001207-300A REV 0.0

REVISED: Thu Aug 16 20:53:43 1990

ABBR: CBPR

ENGR: GOLENBIESKI

PAGE: 16 of 21

8

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DUPONT-204
CPU OR I/O BAY BACKPLANE TYPE
J11 1P

TOP
3
2
1
0
5
4
BOTTOM

SIGNAL
SIGNAL
GROUND
SIGNAL
GROUND

GROUND ALL PINS
ON THESE TWO ROWS

201	MB1_XRE.RD_DATA<16>
202	MB1_XRE.RD_DATA<17>
203	MB1_XRE.RD_DATA<24>
204	MB1_XRE.RD_DATA<25>
205	MB1_XRE.RD_PAR<2>
206	MB1_XRE.RD_PAR<3>
207	XSE_MBI.ADDR<22>
208	XSE_MBI.ADDR<23>
209	XSE_MBI.ADDR<24>
210	XSE_MBI.ADDR<25>
211	XSE_MBI.ADDR<26>
212	XSE_MBI.ADDR<27>
213	XSE_MBI.ADDR<28>
214	XSE_MBI.CTL_PAR<4>
215	XSE_MBI.WR_PAR<2>
216	XSE_MBI.WR_PAR<3>
217	XSE_MBI.WR_ZONE<2>
218	XSE_MBI.WR_ZONE<3>
219	MB1_XSIE.SEND_PAR_ERR
220	XSIE_MBI.SPARE0
221	XSIE_MBI.SPARE1
222	XS0E_MBI.SPARE0
223	XS0E_MBI.SPARE1
224	MB1_XRE.SPARE0
225	MB1_XRE.SPARE1
226	XC_SPI.SPARE2
227	SPI_XC.HW_HUNG
228	XRE_SPI.SPARE0
229	XRE_SPI.SPARE1
230	SPI_XS0E.SPARE0
231	SPI_XS0E.SPARE1
232	SPI_XSIE.SPARE0
233	SPI_XSIE.SPARE1
234	SPI_XSE.CTL_PAR<4>
235	SPI_XSE.WR_PAR<2>
236	SPI_XSE.WR_PAR<3>
237	SPI_XSE.WR_ZONE<2>
238	SPI_XSE.WR_ZONE<3>
239	SPI_XSE.ADDR<22>
240	SPI_XSE.ADDR<23>
241	SPI_XSE.ADDR<24>
242	SPI_XSE.ADDR<25>
243	SPI_XSE.ADDR<26>
244	SPI_XSE.ADDR<27>
245	SPI_XSE.ADDR<28>
246	XRE_SPI.RD_DATA<16>
247	XRE_SPI.RD_DATA<17>
248	XRE_SPI.RD_DATA<24>
249	XRE_SPI.RD_DATA<25>
250	XRE_SPI.RD_PAR<2>
251	XRE_SPI.RD_PAR<3>

301	MB1_XRO.RD_DATA<16>
302	MB1_XRO.RD_DATA<17>
303	MB1_XRO.RD_DATA<24>
304	MB1_XRO.RD_DATA<25>
305	MB1_XRO.RD_PAR<2>
306	MB1_XRO.RD_PAR<3>
307	XSO_MBI.ADDR<22>
308	XSO_MBI.ADDR<23>
309	XSO_MBI.ADDR<24>
310	XSO_MBI.ADDR<25>
311	XSO_MBI.ADDR<26>
312	XSO_MBI.ADDR<27>
313	XSO_MBI.ADDR<28>
314	XSO_MBI.CTL_PAR<4>
315	XSO_MBI.WR_PAR<2>
316	XSO_MBI.WR_PAR<3>
317	XSO_MBI.WR_ZONE<2>
318	XSO_MBI.WR_ZONE<3>
319	MB1_XSIO.SEND_PAR_ERR
320	XSIO_MBI.SPARE0
321	XSIO_MBI.SPARE1
322	XS0O_MBI.SPARE0
323	XS0O_MBI.SPARE1
324	MB1_XRO.SPARE0
325	MB1_XRO.SPARE1
326	XC_SPI.SPARE0
327	XC_SPI.SPARE1
328	XRO_SPI.SPARE0
329	XRO_SPI.SPARE1
330	SPI_XS0O.SPARE0
331	SPI_XS0O.SPARE1
332	SPI_XSIO.SPARE0
333	SPI_XSIO.SPARE1
334	SPI_XSO.CTL_PAR<4>
335	SPI_XSO.WR_PAR<2>
336	SPI_XSO.WR_PAR<3>
337	SPI_XSO.WR_ZONE<2>
338	SPI_XSO.WR_ZONE<3>
339	SPI_XSO.ADDR<22>
340	SPI_XSO.ADDR<23>
341	SPI_XSO.ADDR<24>
342	SPI_XSO.ADDR<25>
343	SPI_XSO.ADDR<26>
344	SPI_XSO.ADDR<27>
345	SPI_XSO.ADDR<28>
346	XRO_SPI.RD_DATA<16>
347	XRO_SPI.RD_DATA<17>
348	XRO_SPI.RD_DATA<24>
349	XRO_SPI.RD_DATA<25>
350	XRO_SPI.RD_PAR<2>
351	XRO_SPI.RD_PAR<3>

501	MB1_XRE.RD_RDY
502	MB1_XRE.RD_PAR<0>
503	MB1_XRE.RD_PAR<1>
504	MB1_XRE.RD_DATA<0>
505	MB1_XRE.RD_DATA<1>
506	MB1_XRE.RD_DATA<8>
507	MB1_XRE.RD_DATA<9>
508	XSE_MBI.WR_ZONE<0>
509	XSE_MBI.WR_ZONE<1>
510	XSE_MBI.WR_PAR<0>
511	XSE_MBI.WR_PAR<1>
512	XSE_MBI.WR_DATA<0>
513	XSE_MBI.WR_DATA<1>
514	XSE_MBI.WR_DATA<8>
515	XSE_MBI.WR_DATA<9>
516	XSE_MBI.WR_DATA<2>
517	XSE_MBI.WR_DATA<3>
518	XSE_MBI.WR_DATA<4>
519	XSE_MBI.WR_DATA<10>
520	XC_MBI.SCAN_CTL<0>
521	XC_MBI.SCAN_CTL<1>
522	MB1_XRE.RD_DATA<2>
523	MB1_XRE.RD_DATA<3>
524	MB1_XRE.RD_DATA<4>
525	MB1_XRE.RD_DATA<10>
526	MB1_XRE.RD_DATA<11>
527	MB1_XRE.RD_DATA<12>
528	MB1_XRE.RD_DATA<5>
529	MB1_XRE.RD_DATA<6>
530	XC_SPI.SCAN_CTL<0>
531	XC_SPI.SCAN_CTL<1>
532	SPI_XSE.WR_ZONE<0>
533	SPI_XSE.WR_ZONE<1>
534	SPI_XSE.WR_PAR<0>
535	SPI_XSE.WR_PAR<1>
536	SPI_XSE.WR_DATA<0>
537	XRE_SPI.RD_RDY
538	XRE_SPI.RD_PAR<0>
539	XRE_SPI.RD_PAR<1>
540	XRE_SPI.RD_DATA<0>
541	XRE_SPI.RD_DATA<1>
542	XRE_SPI.RD_DATA<8>
543	XRE_SPI.RD_DATA<9>
544	SPI_XRE.RTN_PAR_ERR
545	
546	
547	
548	
549	
550	BP_BP.PORTID_I<2>
551	BP_BP.PORTID_I<3>

601	MB1_XRO.RD_RDY
602	MB1_XRO.RD_PAR<0>
603	MB1_XRO.RD_PAR<1>
604	MB1_XRO.RD_DATA<0>
605	MB1_XRO.RD_DATA<1>
606	MB1_XRO.RD_DATA<8>
607	MB1_XRO.RD_DATA<9>
608	XSO_MBI.WR_ZONE<0>
609	XSO_MBI.WR_ZONE<1>
610	XSO_MBI.WR_PAR<0>
611	XSO_MBI.WR_PAR<1>
612	XSO_MBI.WR_DATA<0>
613	XSO_MBI.WR_DATA<1>
614	XSO_MBI.WR_DATA<8>
615	XSO_MBI.WR_DATA<9>
616	XSO_MBI.WR_DATA<2>
617	XSO_MBI.WR_DATA<3>
618	XSO_MBI.WR_DATA<4>
619	XSO_MBI.WR_DATA<10>
620	MB1_XC.HARD_ERROR
621	
622	MB1_XRO.RD_DATA<2>
623	MB1_XRO.RD_DATA<3>
624	MB1_XRO.RD_DATA<4>
625	MB1_XRO.RD_DATA<10>
626	MB1_XRO.RD_DATA<11>
627	MB1_XRO.RD_DATA<12>
628	MB1_XRO.RD_DATA<5>
629	MB1_XRO.RD_DATA<6>
630	XC_UPI.SCAN_CTL<0>
631	XC_UPI.SCAN_CTL<1>
632	SPI_XSO.WR_ZONE<0>
633	SPI_XSO.WR_ZONE<1>
634	SPI_XSO.WR_PAR<0>
635	SPI_XSO.WR_PAR<1>
636	SPI_XSO.WR_DATA<0>
637	XRO_SPI.RD_RDY
638	XRO_SPI.RD_PAR<0>
639	XRO_SPI.RD_PAR<1>
640	XRO_SPI.RD_DATA<0>
641	XRO_SPI.RD_DATA<1>
642	XRO_SPI.RD_DATA<8>
643	XRO_SPI.RD_DATA<9>
644	SPI_XRO.RTN_PAR_ERR
645	XC_UPI.SCAN_CTL<2>
646	
647	
648	SPI_XC.SOFT_ERROR
649	XC_IAP.RESET
650	BP_BP.PORTID_I<0>
651	BP_BP.PORTID_I<1>

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TITLE: CBPR
DRAWING: 411-000252-300A Rev 0.0

ABBR: CBPR
ENGR: GOLENBIESKI

REVISED: Fri Aug 17 09:34:51 1990

PAGE: 17 OF 21

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DUPONT-204
CPU OR I/O BAY BACKPLANE TYPE
J12 1P

TOP

3 SIGNAL
2 SIGNAL
1 GROUND
6 SIGNAL
5 SIGNAL
4 GROUND

BOTTOM

GROUND ALL PINS
ON THESE TWO ROWS!

201	MB1_XRE.RD_DATA<30>
202	MB1_XRE.RD_DATA<31>
203	MB1_XRE.RD_DATA<18>
204	MB1_XRE.RD_DATA<19>
205	MB1_XRE.RD_DATA<20>
206	MB1_XRE.RD_DATA<26>
207	MB1_XRE.RD_DATA<27>
208	MB1_XRE.RD_DATA<28>
209	XSE_MBI.ADDR<15>
210	XSE_MBI.ADDR<16>
211	XSE_MBI.ADDR<17>
212	XSE_MBI.ADDR<18>
213	XSE_MBI.ADDR<19>
214	XSE_MBI.ADDR<20>
215	XSE_MBI.ADDR<21>
216	XSE_MBI.WR_DATA<26>
217	XSE_MBI.WR_DATA<27>
218	XSE_MBI.WR_DATA<28>
219	XSE_MBI.WR_DATA<16>
220	XSE_MBI.WR_DATA<17>
221	XSE_MBI.WR_DATA<24>
222	XSE_MBI.WR_DATA<25>
223	
224	XC_IAI.CCU_CNTRL_ENA
225	XC_SPI.SLOG_ENA
226	XC_IAI.CCU_RBE<2>
227	XC_IAI.CCU_RBE<3>
228	NC
229	NC
230	SPI_XSE.WR_DATA<26>
231	SPI_XSE.WR_DATA<27>
232	SPI_XSE.WR_DATA<28>
233	SPI_XSE.WR_DATA<16>
234	SPI_XSE.WR_DATA<17>
235	SPI_XSE.WR_DATA<24>
236	SPI_XSE.WR_DATA<25>
237	SPI_XSE.ADDR<15>
238	SPI_XSE.ADDR<16>
239	SPI_XSE.ADDR<17>
240	SPI_XSE.ADDR<18>
241	SPI_XSE.ADDR<19>
242	SPI_XSE.ADDR<20>
243	SPI_XSE.ADDR<21>
244	XRE_SPI.RD_DATA<30>
245	XRE_SPI.RD_DATA<31>
246	XRE_SPI.RD_DATA<18>
247	XRE_SPI.RD_DATA<19>
248	XRE_SPI.RD_DATA<20>
249	XRE_SPI.RD_DATA<26>
250	XRE_SPI.RD_DATA<27>
251	XRE_SPI.RD_DATA<28>

301	MB1_XRO.RD_DATA<30>
302	MB1_XRO.RD_DATA<31>
303	MB1_XRO.RD_DATA<18>
304	MB1_XRO.RD_DATA<19>
305	MB1_XRO.RD_DATA<20>
306	MB1_XRO.RD_DATA<26>
307	MB1_XRO.RD_DATA<27>
308	MB1_XRO.RD_DATA<28>
309	XSO_MBI.ADDR<15>
310	XSO_MBI.ADDR<16>
311	XSO_MBI.ADDR<17>
312	XSO_MBI.ADDR<18>
313	XSO_MBI.ADDR<19>
314	XSO_MBI.ADDR<20>
315	XSO_MBI.ADDR<21>
316	XSO_MBI.WR_DATA<26>
317	XSO_MBI.WR_DATA<27>
318	XSO_MBI.WR_DATA<28>
319	XSO_MBI.WR_DATA<16>
320	XSO_MBI.WR_DATA<17>
321	XSO_MBI.WR_DATA<24>
322	XSO_MBI.WR_DATA<25>
323	
324	XC_IAI.CLOCK_SYNC
325	XC_IAI.CCU_CLEAR
326	XC_IAI.CCU_RBE<0>
327	XC_IAI.CCU_RBE<1>
328	NC
329	NC
330	SPI_XSO.WR_DATA<26>
331	SPI_XSO.WR_DATA<27>
332	SPI_XSO.WR_DATA<28>
333	SPI_XSO.WR_DATA<16>
334	SPI_XSO.WR_DATA<17>
335	SPI_XSO.WR_DATA<24>
336	SPI_XSO.WR_DATA<25>
337	SPI_XSO.ADDR<15>
338	SPI_XSO.ADDR<16>
339	SPI_XSO.ADDR<17>
340	SPI_XSO.ADDR<18>
341	SPI_XSO.ADDR<19>
342	SPI_XSO.ADDR<20>
343	SPI_XSO.ADDR<21>
344	XRO_SPI.RD_DATA<30>
345	XRO_SPI.RD_DATA<31>
346	XRO_SPI.RD_DATA<18>
347	XRO_SPI.RD_DATA<19>
348	XRO_SPI.RD_DATA<20>
349	XRO_SPI.RD_DATA<26>
350	XRO_SPI.RD_DATA<27>
351	XRO_SPI.RD_DATA<28>

501	MB1_XSOE.SEND_PAR_ERR
502	MB1_XSE.BANK_DONE<0>
503	MB1_XSE.BANK_DONE<1>
504	MB1_XSE.BANK_DONE<2>
505	MB1_XSE.BANK_DONE<3>
506	MB1_XSE.BANK_DONE<4>
507	MB1_XSE.BANK_DONE<5>
508	MB1_XSE.BANK_DONE<6>
509	MB1_XSE.BANK_DONE<7>
510	MB1_XSE.BANK_DONE<8>
511	MB1_XSE.BANK_DONE<9>
512	MB1_XSE.BANK_DONE<10>
513	MB1_XSE.BANK_DONE<11>
514	MB1_XSE.BANK_DONE<12>
515	MB1_XSE.BANK_DONE<13>
516	MB1_XSE.BANK_DONE<14>
517	MB1_XSE.BANK_DONE<15>
518	
519	XSE_MBI.REF_REQ
520	XSE_MBI.RDY
521	XC_MBI.SCAN_CTL<2>
522	XC_SPI.CU_STATUS
523	SPI_XC.DEADLOCK
524	SPI_XC.TRAP_COMP
525	XC_SPI.TRAP_TYPE<2>
526	XC_SPI.TRAP_TYPE<3>
527	XC_SPI.TRAP_VECT<6>
528	XC_SPI.TRAP_VECT<7>
529	XC_SPI.TRAP_VECT<8>
530	XC_SPI.TRAP_VECT<9>
531	XC_SPI.TRAP_VECT<10>
532	XC_SPI.TRAP_VECT<11>
533	XC_SPI.USEC_EN
534	SPI_XSE.WR_DATA<1>
535	SPI_XSE.WR_DATA<8>
536	SPI_XSE.WR_DATA<9>
537	SPI_XSE.WR_DATA<2>
538	SPI_XSE.WR_DATA<3>
539	SPI_XSE.WR_DATA<4>
540	SPI_XSE.WR_DATA<10>
541	XSE_SPI.A_ST_PEND
542	XSE_SPI.A_REQ_PEND
543	XSE_SPI.B_REQ_NEXT
544	XRE_SPI.RD_DATA<2>
545	XRE_SPI.RD_DATA<3>
546	XRE_SPI.RD_DATA<4>
547	XRE_SPI.RD_DATA<10>
548	XRE_SPI.RD_DATA<11>
549	XRE_SPI.RD_DATA<12>
550	XRE_SPI.RD_DATA<5>
551	XRE_SPI.RD_DATA<6>

601	MB1_XSOE.SEND_PAR_ERR
602	MB1_XSO.BANK_DONE<0>
603	MB1_XSO.BANK_DONE<1>
604	MB1_XSO.BANK_DONE<2>
605	MB1_XSO.BANK_DONE<3>
606	MB1_XSO.BANK_DONE<4>
607	MB1_XSO.BANK_DONE<5>
608	MB1_XSO.BANK_DONE<6>
609	MB1_XSO.BANK_DONE<7>
610	MB1_XSO.BANK_DONE<8>
611	MB1_XSO.BANK_DONE<9>
612	MB1_XSO.BANK_DONE<10>
613	MB1_XSO.BANK_DONE<11>
614	MB1_XSO.BANK_DONE<12>
615	MB1_XSO.BANK_DONE<13>
616	MB1_XSO.BANK_DONE<14>
617	MB1_XSO.BANK_DONE<15>
618	XSO_MBI.REF_REQ
619	XSO_MBI.RDY
620	XC_SPI.SCAN_CTL<2>
621	SPI_XC.HARD_ERROR
622	XC_SPI.CU_STATUS_EN
623	XC_SPI.MT_COMP
624	XC_SPI.TRAP_RDY
625	XC_SPI.TRAP_TYPE<0>
626	XC_SPI.TRAP_TYPE<1>
627	UPI_XC.HARD_ERROR
628	XC_SPI.TRAP_VECT<0>
629	XC_SPI.TRAP_VECT<1>
630	XC_SPI.TRAP_VECT<2>
631	XC_SPI.TRAP_VECT<3>
632	XC_SPI.TRAP_VECT<4>
633	XC_SPI.TRAP_VECT<5>
634	SPI_XSO.WR_DATA<1>
635	SPI_XSO.WR_DATA<8>
636	SPI_XSO.WR_DATA<9>
637	SPI_XSO.WR_DATA<2>
638	SPI_XSO.WR_DATA<3>
639	SPI_XSO.WR_DATA<4>
640	SPI_XSO.WR_DATA<10>
641	XSO_SPI.A_ST_PEND
642	XSO_SPI.A_REQ_PEND
643	XSO_SPI.B_REQ_NEXT
644	XRO_SPI.RD_DATA<2>
645	XRO_SPI.RD_DATA<3>
646	XRO_SPI.RD_DATA<4>
647	XRO_SPI.RD_DATA<10>
648	XRO_SPI.RD_DATA<11>
649	XRO_SPI.RD_DATA<12>
650	XRO_SPI.RD_DATA<5>
651	XRO_SPI.RD_DATA<6>

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TITLE: CBPR
DRAWING: 411-000252-300A Rev 0.0
REVISED: Fri Aug 17 09:36:41 1990

ABBR: CBPR
ENGR: GOLENBIESKI

PAGE: 18 OF 21

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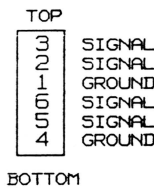
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DUPONT-204
CPU OR I/O BAY BACKPLANE TYPE
J13 1P



GROUND ALL PINS
ON THESE TWO ROWS!

201	XSE_MBI.ADDR<5>
202	XSE_MBI.ADDR<6>
203	XSE_MBI.CYCLE<1>
204	XSE_MBI.ADDR<3>
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214	XSE_MBI.WR_DATA<15>
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216	XSE_MBI.WR_DATA<22>
217	XSE_MBI.WR_DATA<23>
218	XSE_MBI.WR_DATA<29>
219	XSE_MBI.WR_DATA<30>
220	XSE_MBI.WR_DATA<31>
221	XSE_MBI.CTL_PAR<2>
222	XSE_MBI.CTL_PAR<3>
223	XSE_MBI.WR_DATA<18>
224	XSE_MBI.WR_DATA<19>
225	XSE_MBI.WR_DATA<20>
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228	SPI_XSE.WR_DATA<15>
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310	XSO_MBI.ADDR<12>
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314	XSO_MBI.WR_DATA<15>
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316	XSO_MBI.WR_DATA<22>
317	XSO_MBI.WR_DATA<23>
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320	XSO_MBI.WR_DATA<31>
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322	XSO_MBI.CTL_PAR<3>
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324	XSO_MBI.WR_DATA<19>
325	XSO_MBI.WR_DATA<20>
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328	SPI_XSO.WR_DATA<15>
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502	MB1_XRE.RD_DATA<13>
503	MB1_XRE.RD_DATA<14>
504	MB1_XRE.RD_DATA<15>
505	MB1_XRE.RD_DATA<21>
506	MB1_XRE.RD_DATA<22>
507	MB1_XRE.RD_DATA<23>
508	MB1_XRE.RD_DATA<29>
509	XSE_MBI.CYCLE<0>
510	XSE_MBI.ADDR<7>
511	XSE_MBI.WR_DATA<11>
512	XSE_MBI.WR_DATA<12>
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514	XSE_MBI.CTL_PAR<1>
515	XSE_MBI.WR_DATA<5>
516	XSE_MBI.WR_DATA<6>
517	XSE_MBI.WR_DATA<7>
518	XSE_MBI.WR_DATA<13>
519	XC_MBI.SCAN_IN
520	MB1_XC.SOFT_ERROR
521	-XC_MBI.SYS_RUN
522	SPI_XSE.WR_DATA<11>
523	SPI_XSE.WR_DATA<12>
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529	SPI_XSE.WR_DATA<13>
530	SPI_XSE.WR_DATA<14>
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533	SPI_XSE.BD_SEL<2>
534	SPI_XSE.BD_SEL<3>
535	SPI_XSE.RDY
536	XSE_SPI.B_ST_PEND
537	XSE_SPI.B_REQ_PEND
538	XSE_SPI.A_REQ_NEXT
539	SPI_XSE.CYCLE<0>
540	SPI_XSE.ADDR<7>
541	XRE_SPI.RD_DATA<7>
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543	XRE_SPI.RD_DATA<14>
544	XRE_SPI.RD_DATA<15>
545	XRE_SPI.RD_DATA<21>
546	XRE_SPI.RD_DATA<22>
547	XRE_SPI.RD_DATA<23>
548	XRE_SPI.RD_DATA<29>
549	XC_SPI.SCAN_IN
550	SPI_XC.SCAN_OUT
551	SPI_XC.STOP_CNTR

601	MB1_XRO.RD_DATA<7>
602	MB1_XRO.RD_DATA<13>
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604	MB1_XRO.RD_DATA<15>
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607	MB1_XRO.RD_DATA<23>
608	MB1_XRO.RD_DATA<29>
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612	XSO_MBI.WR_DATA<12>
613	XSO_MBI.CTL_PAR<0>
614	XSO_MBI.CTL_PAR<1>
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616	XSO_MBI.WR_DATA<6>
617	XSO_MBI.WR_DATA<7>
618	XSO_MBI.WR_DATA<13>
619	MB1_XC.SCAN_OUT
620	XC_MBI.RAM_RFSH
621	-XC_MBI.LOG_RUN
622	SPI_XSO.WR_DATA<11>
623	SPI_XSO.WR_DATA<12>
624	SPI_XSO.CTL_PAR<0>
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626	SPI_XSO.WR_DATA<5>
627	SPI_XSO.WR_DATA<6>
628	SPI_XSO.WR_DATA<7>
629	SPI_XSO.WR_DATA<13>
630	SPI_XSO.WR_DATA<14>
631	SPI_XSO.BD_SEL<0>
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633	SPI_XSO.BD_SEL<2>
634	SPI_XSO.BD_SEL<3>
635	SPI_XSO.RDY
636	XSO_SPI.B_ST_PEND
637	XSO_SPI.B_REQ_PEND
638	XSO_SPI.A_REQ_NEXT
639	SPI_XSO.CYCLE<0>
640	SPI_XSO.ADDR<7>
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644	XRO_SPI.RD_DATA<15>
645	XRO_SPI.RD_DATA<21>
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647	XRO_SPI.RD_DATA<23>
648	XRO_SPI.RD_DATA<29>
649	XC_UPI.SCAN_IN
650	UPI_XC.SCAN_OUT
651	

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DRAWING: 411-000252-300A Rev 0.0
REVISID: Fri Aug 17 09:37:33 1990
PAGE: 19 OF 21
ABBR: CBPR
ENGR: GOLENBIESKI

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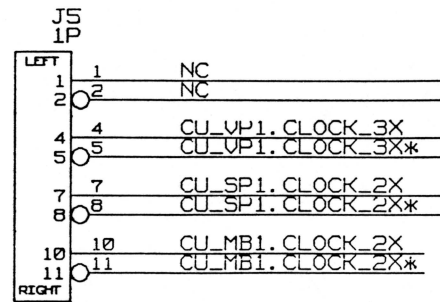
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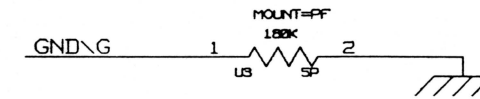
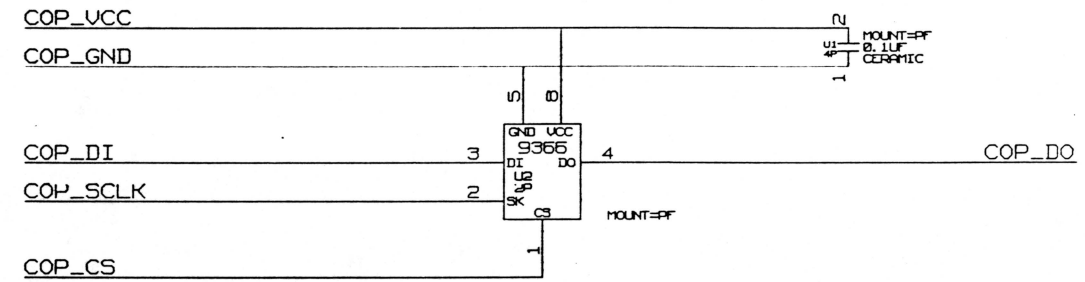
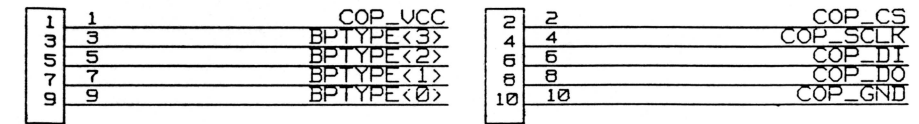
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C3 CLOCK CONNECTOR
 12 PIN STRAIGHT, 3X4 ROW
 (L&R VIEWED FROM INSIDE CARDAGE)

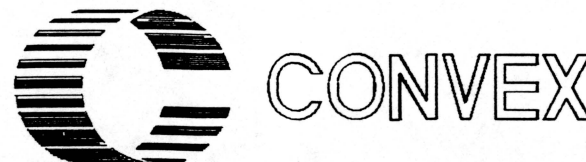


HDR10
 301-000035-004
 MALE-PRESSFIT-STRAIGHT-4 WALL-LONG EJECTOR
 J7 SP



RESISTOR CONNECTS CHASSIS GND TO SIGNAL GND

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 REVISED: Thu Aug 16 20:49:52 1990

ABBR: CBPR
 ENGR: GOLEMBIESKI

PAGE: 20 of 21

SYNONYMS

BP_BP.PORTID_1<3>	12P	BP_MB1.PORTID<3>
BP_BP.PORTID_1<2>	11P	BP_MB1.PORTID<2>
BP_BP.PORTID_1<1>	10P	BP_MB1.PORTID<1>
BP_BP.PORTID_1<0>	9P	BP_MB1.PORTID<0>
BP_BP.PORTID_1<3>	8P	BP_SP1.PORTID<3>
BP_BP.PORTID_1<2>	7P	BP_SP1.PORTID<2>
BP_BP.PORTID_1<1>	6P	BP_SP1.PORTID<1>
BP_BP.PORTID_1<0>	5P	BP_SP1.PORTID<0>
BP_BP.PORTID_1<3>	4P	BP_UP1.PORTID<3>
BP_BP.PORTID_1<2>	3P	BP_UP1.PORTID<2>
BP_BP.PORTID_1<1>	2P	BP_UP1.PORTID<1>
BP_BP.PORTID_1<0>	1P	BP_UP1.PORTID<0>
MB1_BP.LBD_INTL_OUT	29P	BP_MB1.LBD_INTL_IN
SP1_BP.LBD_INTL_OUT	30P	BP_SP1.LBD_INTL_IN
VP1_BP.LBD_INTL_OUT	31P	BP_UP1.LBD_INTL_IN

BPTYPE<3>	21P	COP_GND
BPTYPE<2>	22P	COP_GND
BPTYPE<1>	23P	NC
BPTYPE<0>	24P	NC
CPU RIGHT BPTYPE = 0X3		
BP_MB1.SLOTID<3>	25P	
BP_MB1.SLOTID<2>	26P	GND\G
BP_MB1.SLOTID<1>	27P	
BP_MB1.SLOTID<0>	28P	
MB1 SLOTID = 0XB		
BP_SP1.SLOTID<3>	17P	
BP_SP1.SLOTID<2>	18P	GND\G
BP_SP1.SLOTID<1>	19P	
BP_SP1.SLOTID<0>	20P	GND\G
SP1 SLOTID = 0XA		
BP_UP1.SLOTID<3>	13P	
BP_UP1.SLOTID<2>	14P	GND\G
BP_UP1.SLOTID<1>	15P	GND\G
BP_UP1.SLOTID<0>	16P	
VP1 SLOTID = 0X9		

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ABBR: CBPR
 ENGR: GOLENBIESKI

PAGE: 21 of 21